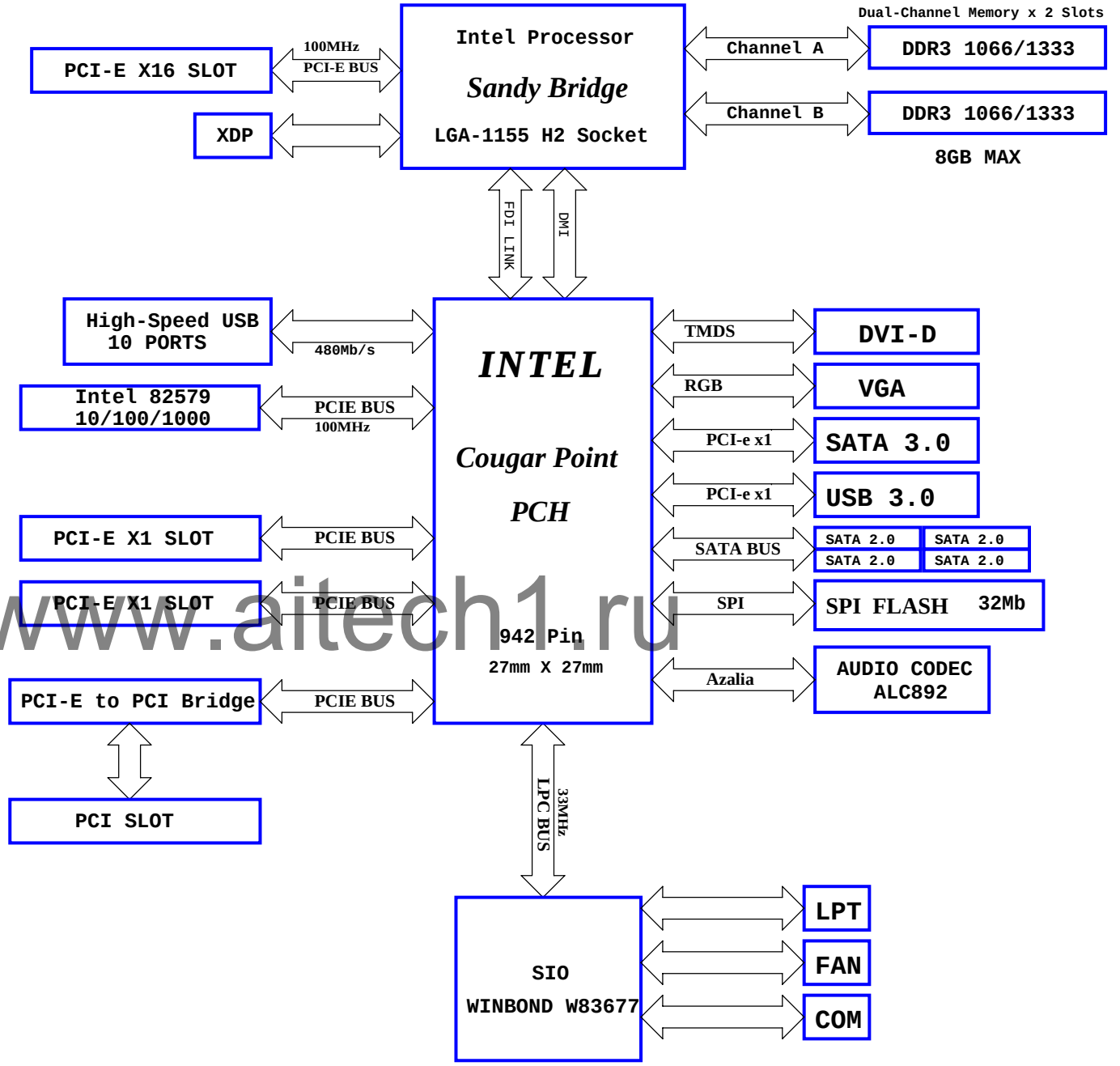
IPM61-BE
Revision: 1.00



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : BLOCK DIAGRAM

Pegatron Corp. Engineer: Livy_Zhu

Size	Project Name	Rev
A3	IPMSB-BE/CR	1.00

Date: Friday, September 24, 2010 Sheet 1 of 83

Schematics Change History

Version	Date	Comments

CAD Note:

Default component footprint is SMD 0402, Y5V, 5% type. Difference footprint show on schematics.

Property: BOM
I = Installed Part.
NI = Not Installed Part.
PROTO = PROTO Phase Only.
VP = Virtual Part.

Schematics Change History

Version	Date	Comments

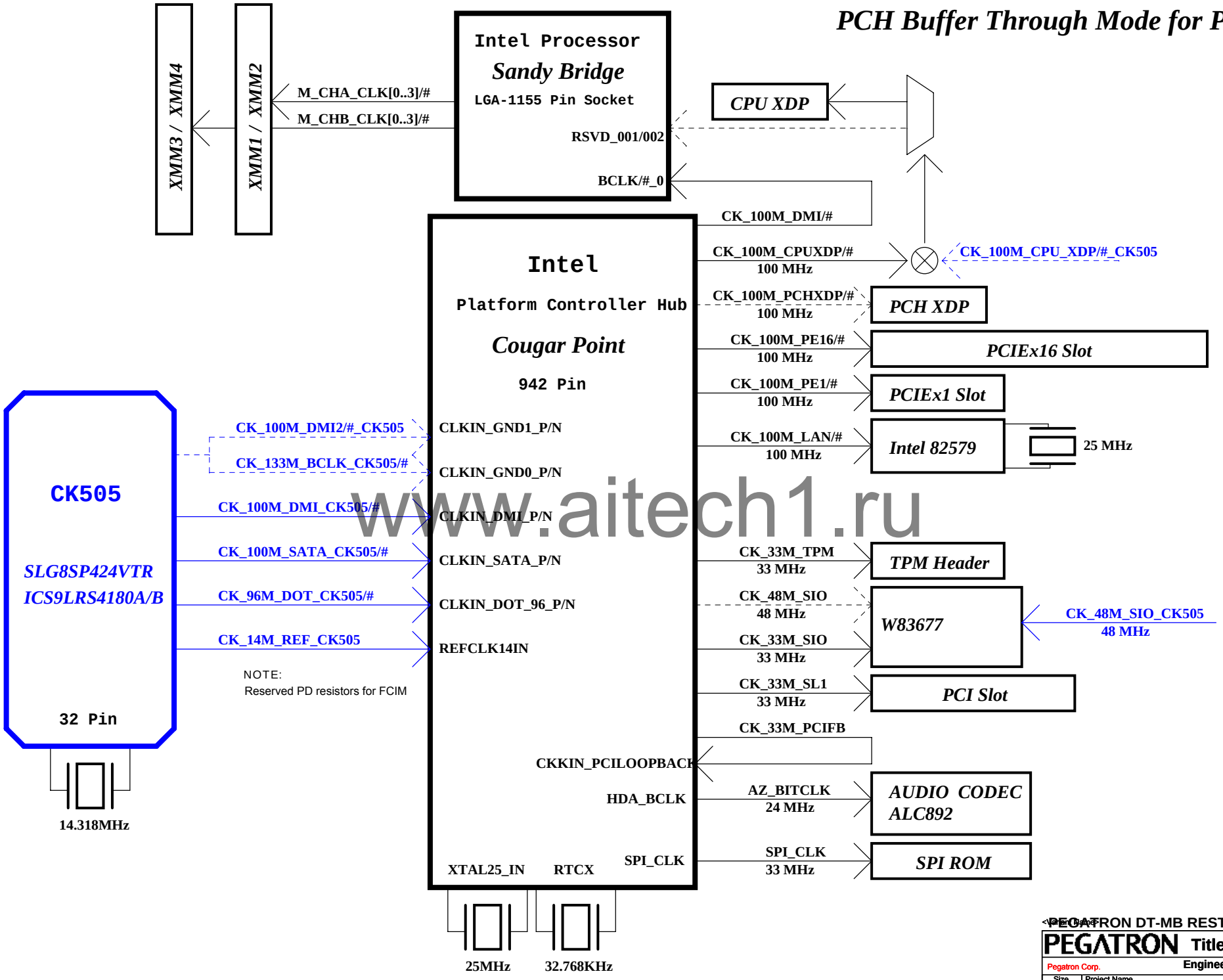
CAD Note:

Default component footprint is SMD 0402, Y5V, 5% type. Difference footprint show on schematics.

Property: BOM
I = Installed Part.
NI = Not Installed Part.

PROTO = PROTO Phase Only.
VP = Virtual Part.

PCH Buffer Through Mode for Pre-Silicon



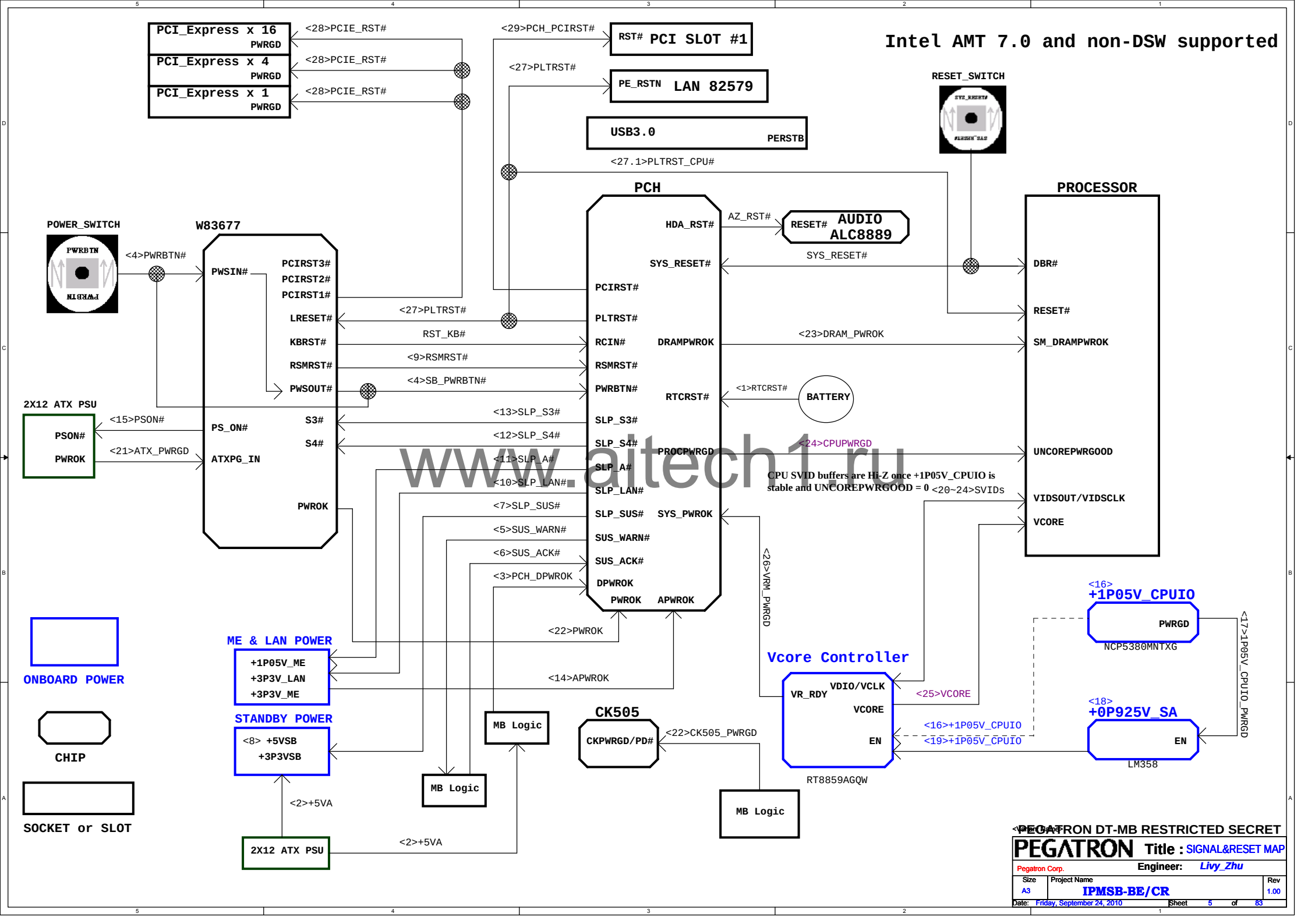
PEGATRON Title : CLCOK DISTRIBUTION

Pegatron Corp. Engineer: Livy_Zhu

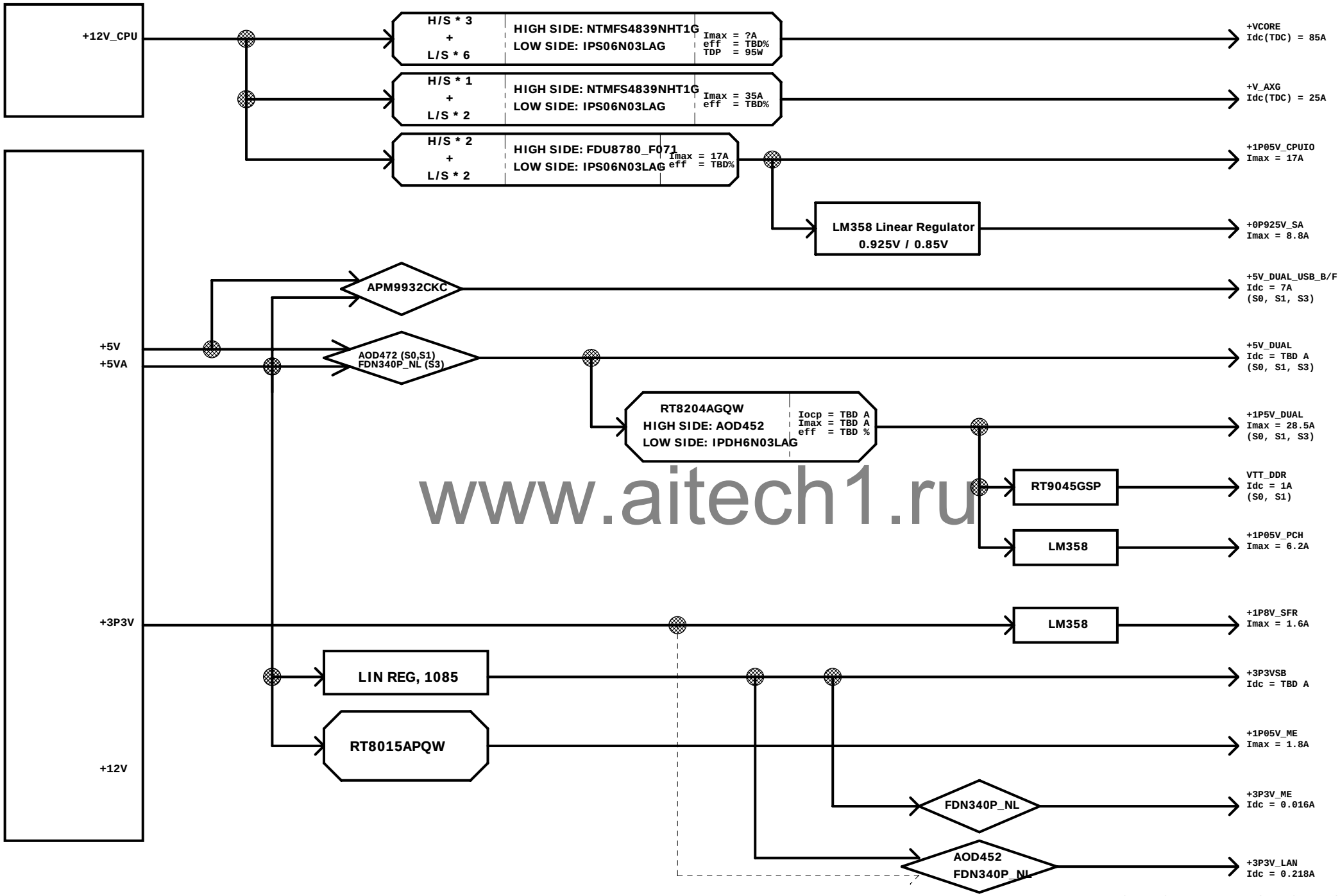
Size	Project Name	Rev
A3	IPMSB-BE/CR	1.00

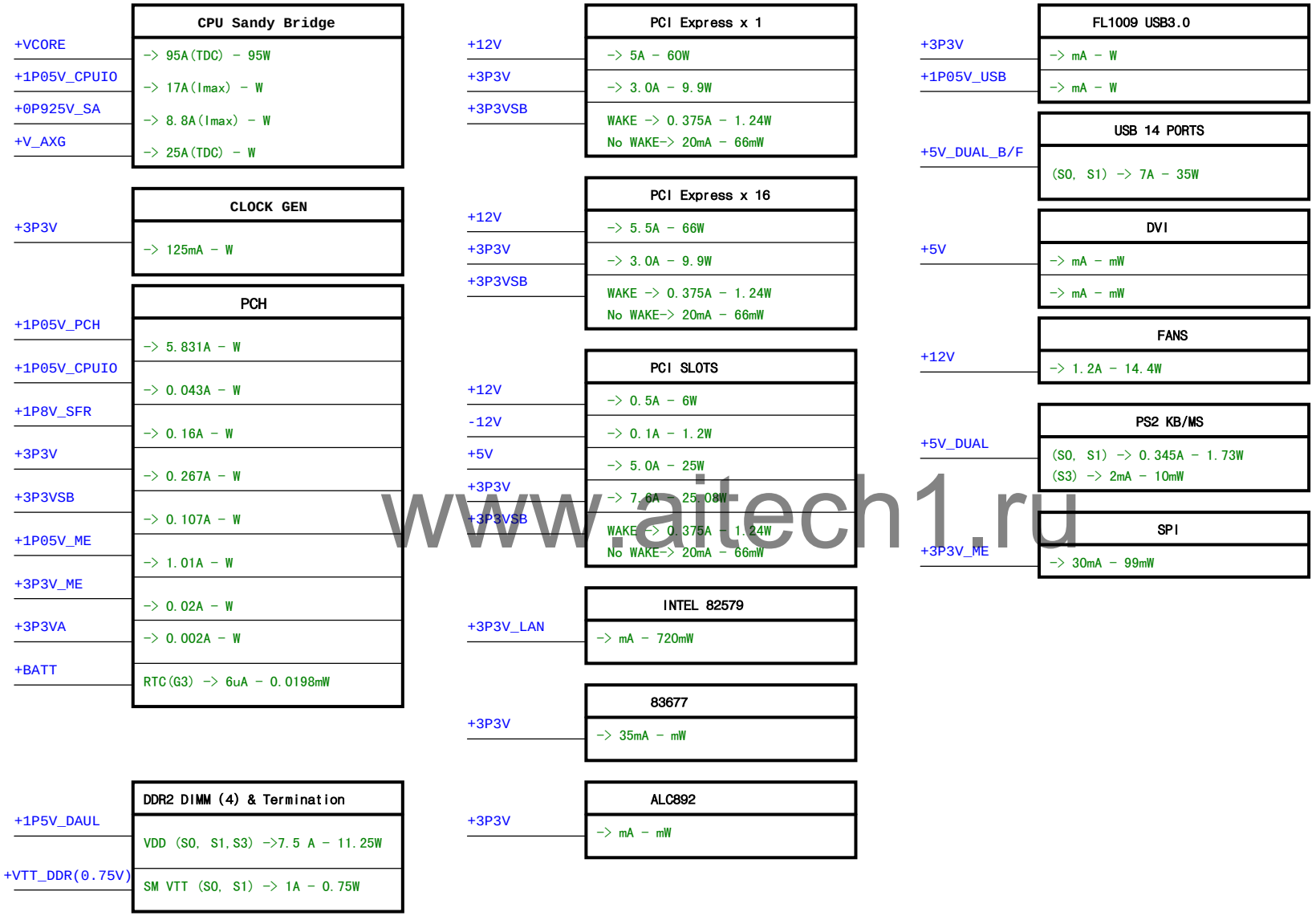
Date: Friday, September 24, 2010 Sheet 4 of 83

Intel AMT 7.0 and non-DSW supported



PEGATRON	Title : SIGNAL&RESET MAP	
Pegatron Corp.	Engineer: Livy_Zhu	
Size: A3	Project Name: IPMSB-BE/CR	Rev: 1.00
Date: Friday, September 24, 2010	Sheet 5 of 83	





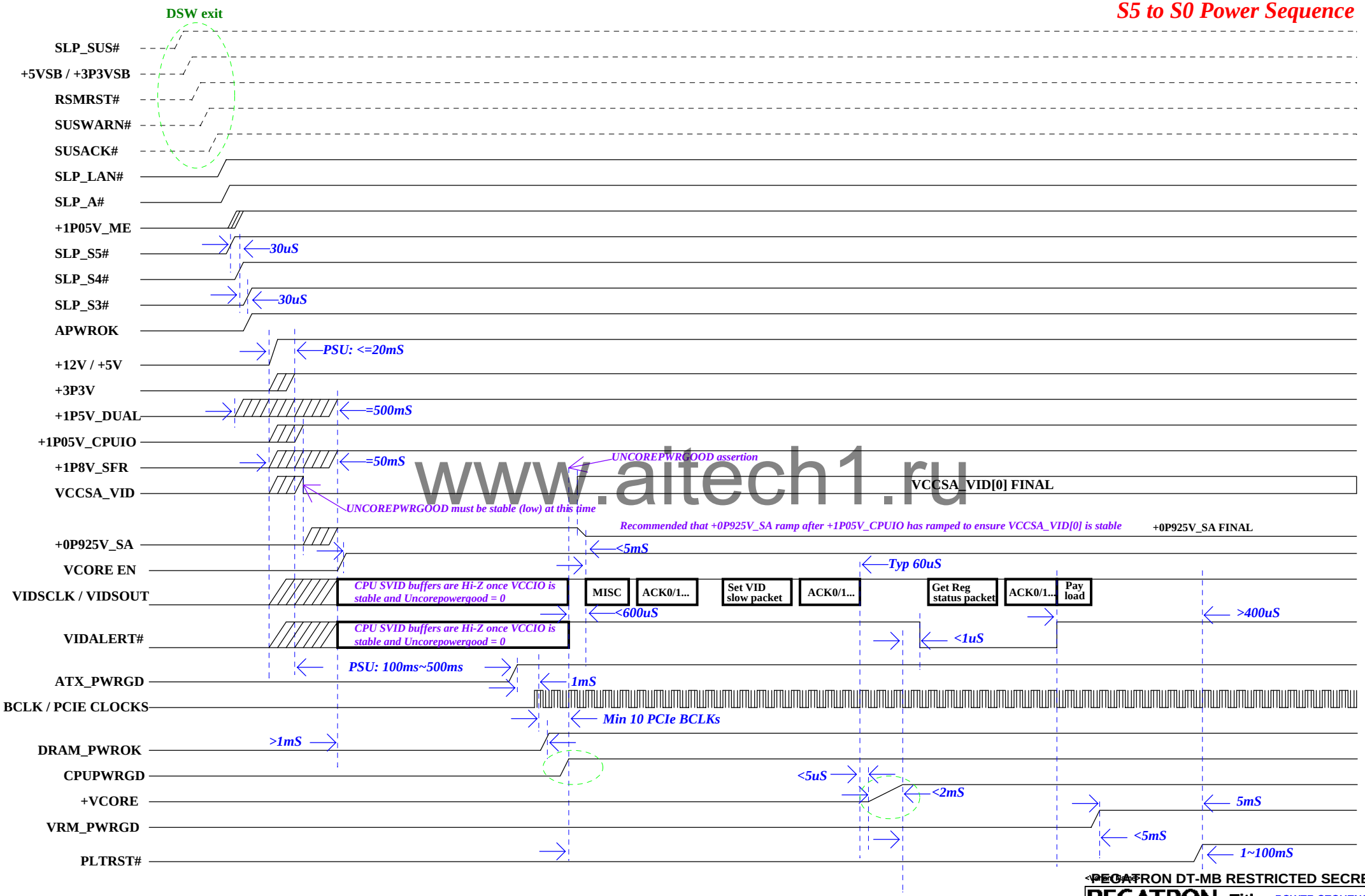
PEGATRON Title : POWER DISTRIBUTION

Pegatron Corp. Engineer: Livy_Zhu

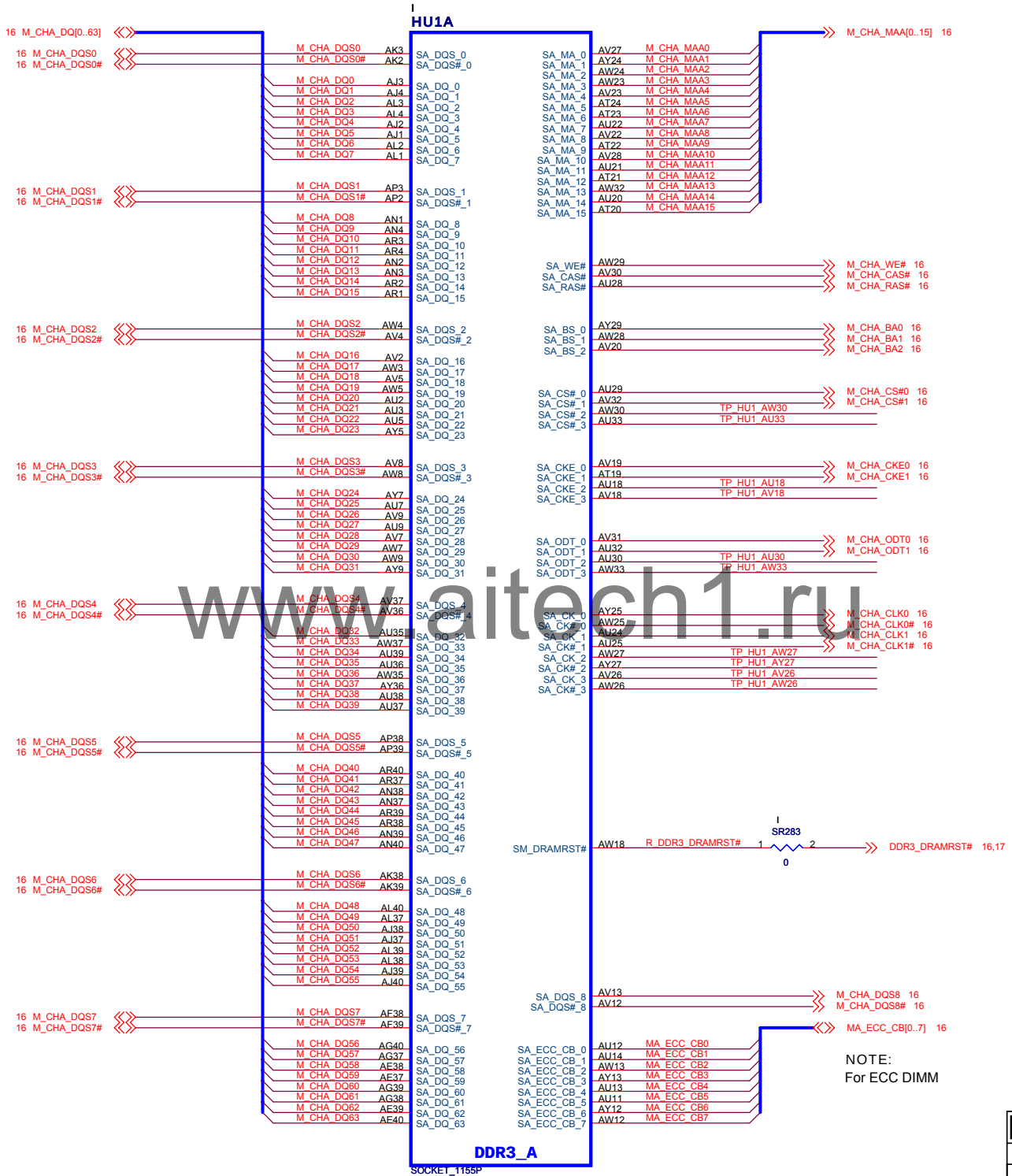
Size	Project Name	Rev
A3	IPMSB-BE/CR	1.00

Date: Friday, September 24, 2010 Sheet 7 of 83

S5 to S0 Power Sequence



PEGATRON	Title : POWER SEQUENCE	
Pegatron Corp.	Engineer: Livy_Zhu	
Size: A3	Project Name: IPMSB-BE/CR	Rev: 1.00
Date: Friday, September 24, 2010	Sheet 8 of 83	



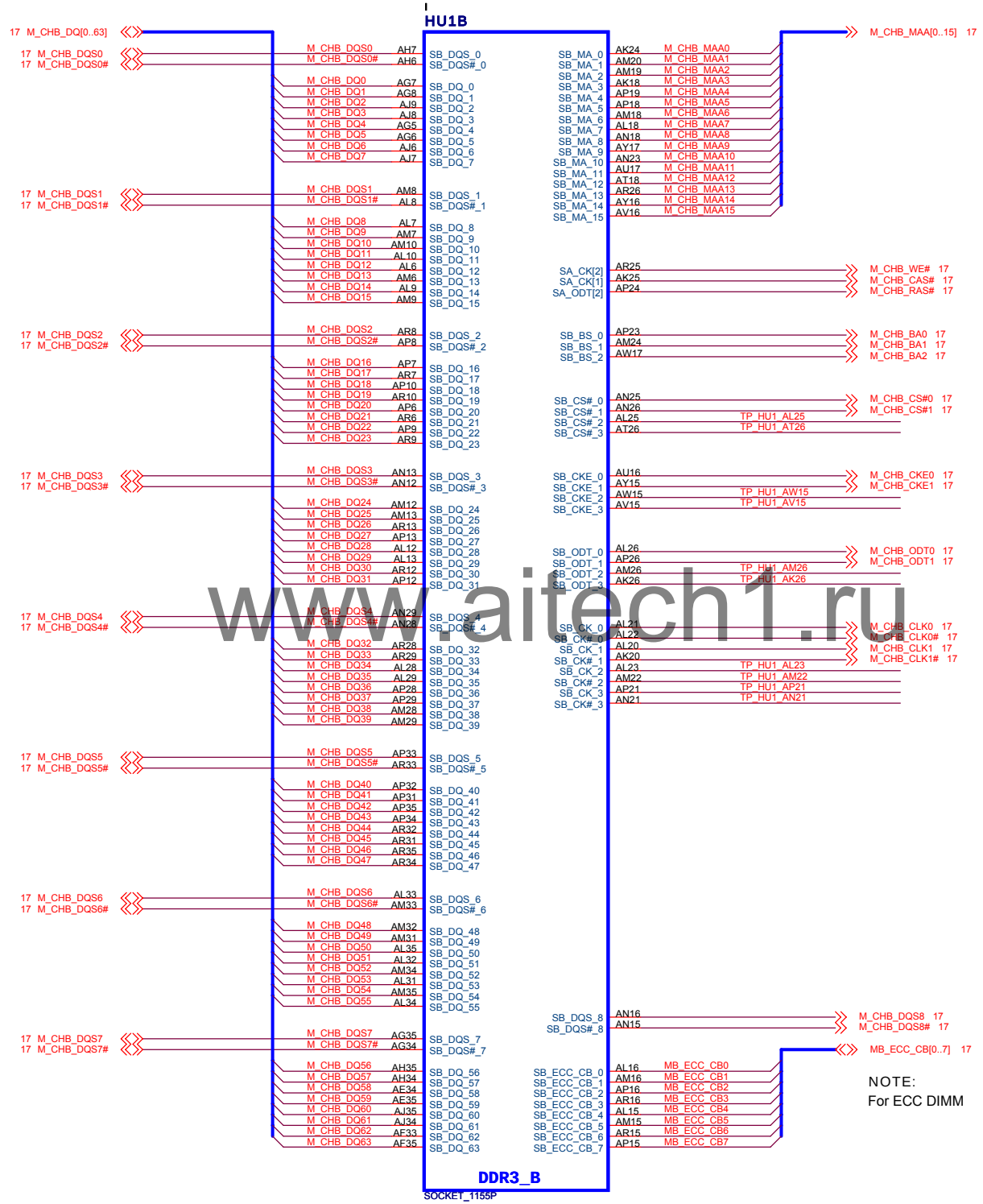
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : DDR3_A 1-6

Pegatron Corp. Engineer: Livy_Zhu

Size	Project Name	Rev
A3	IPMSB-BE/CR	1.00

Date: Friday, September 24, 2010 Sheet 9 of 83



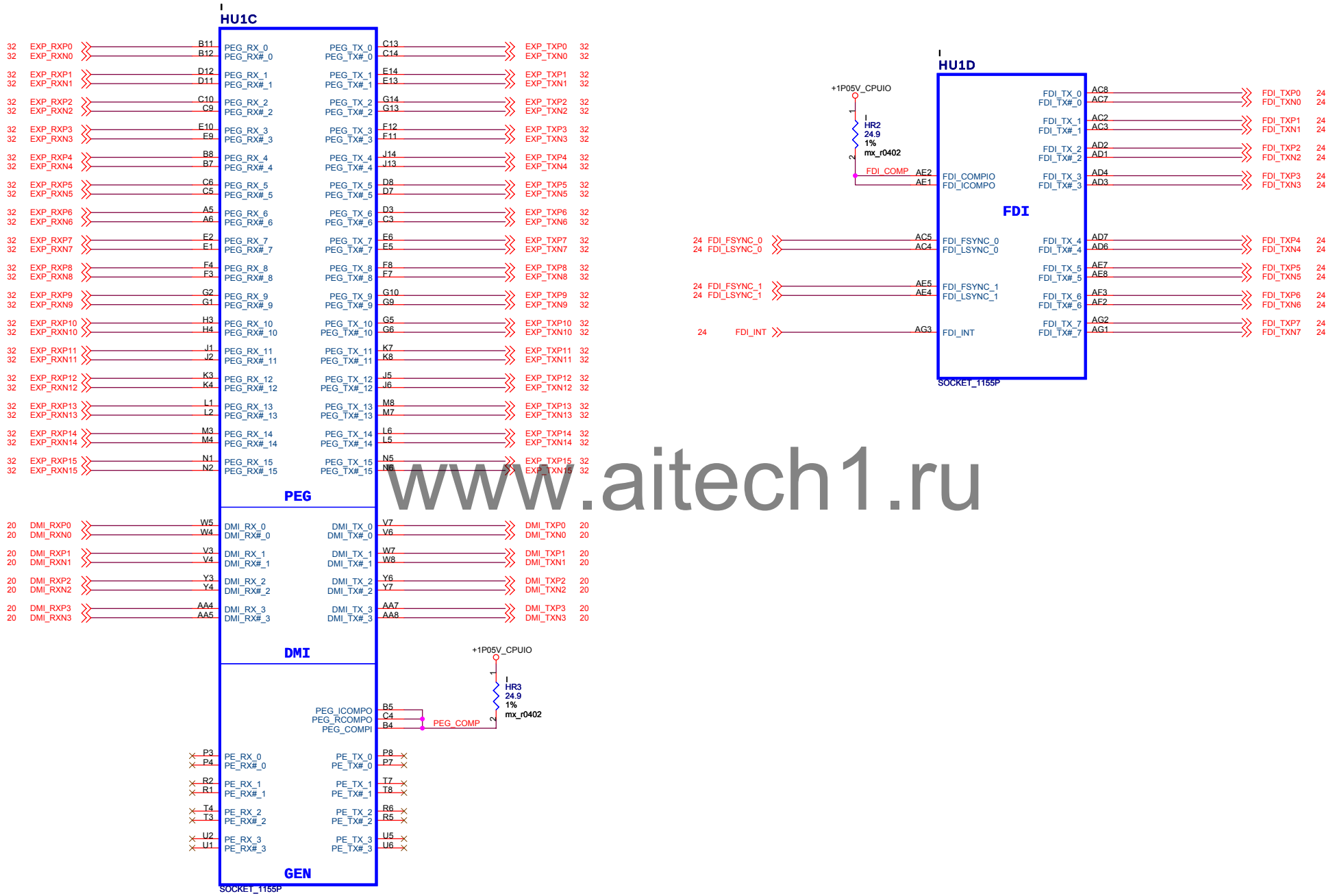
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : DDR3_B 2-6

Pegatron Corp. Engineer: Livy_Zhu

Size	Project Name	Rev
A3	IPMSB-BE/CR	1.00

Date: Friday, September 24, 2010 Sheet 10 of 83

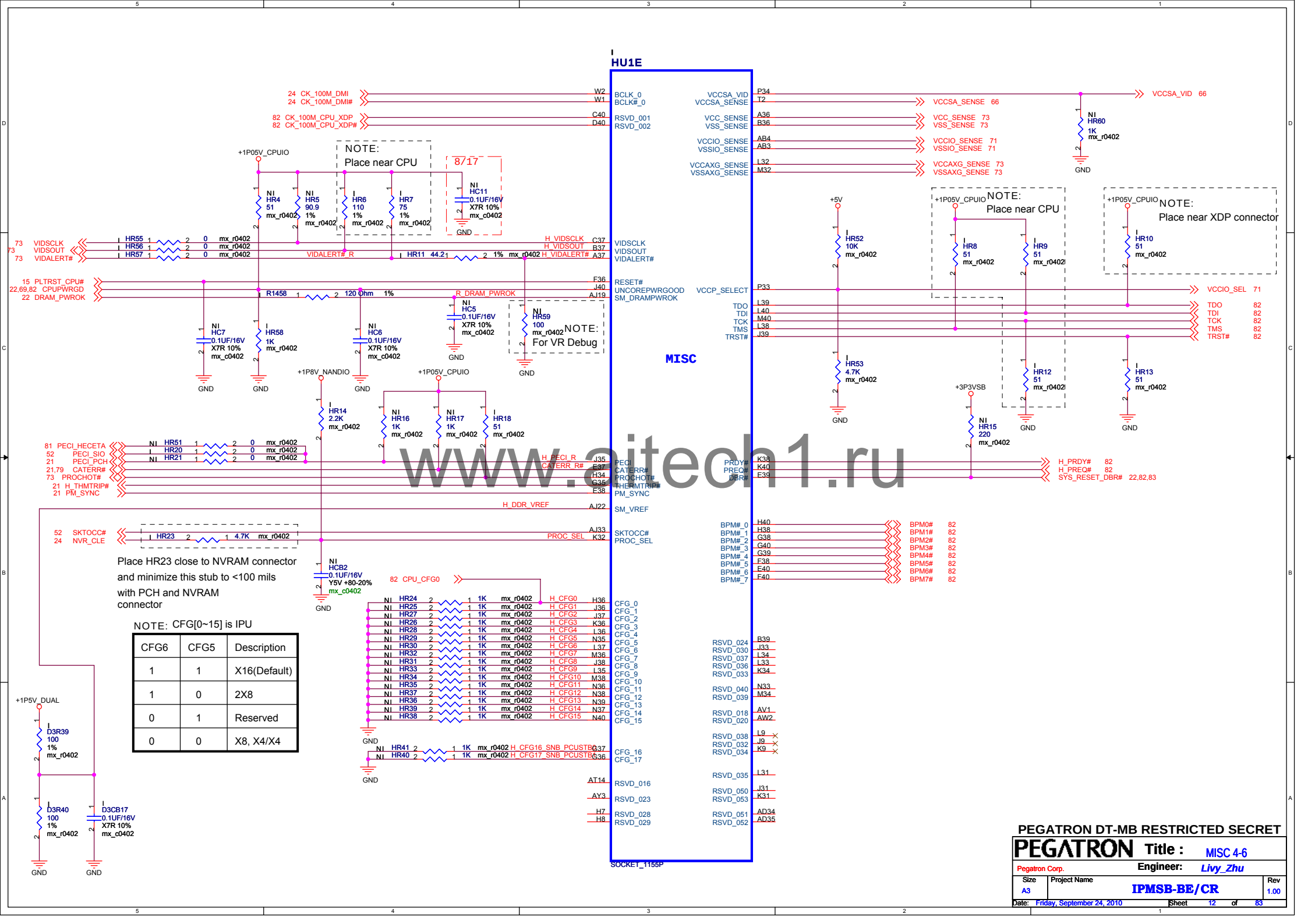


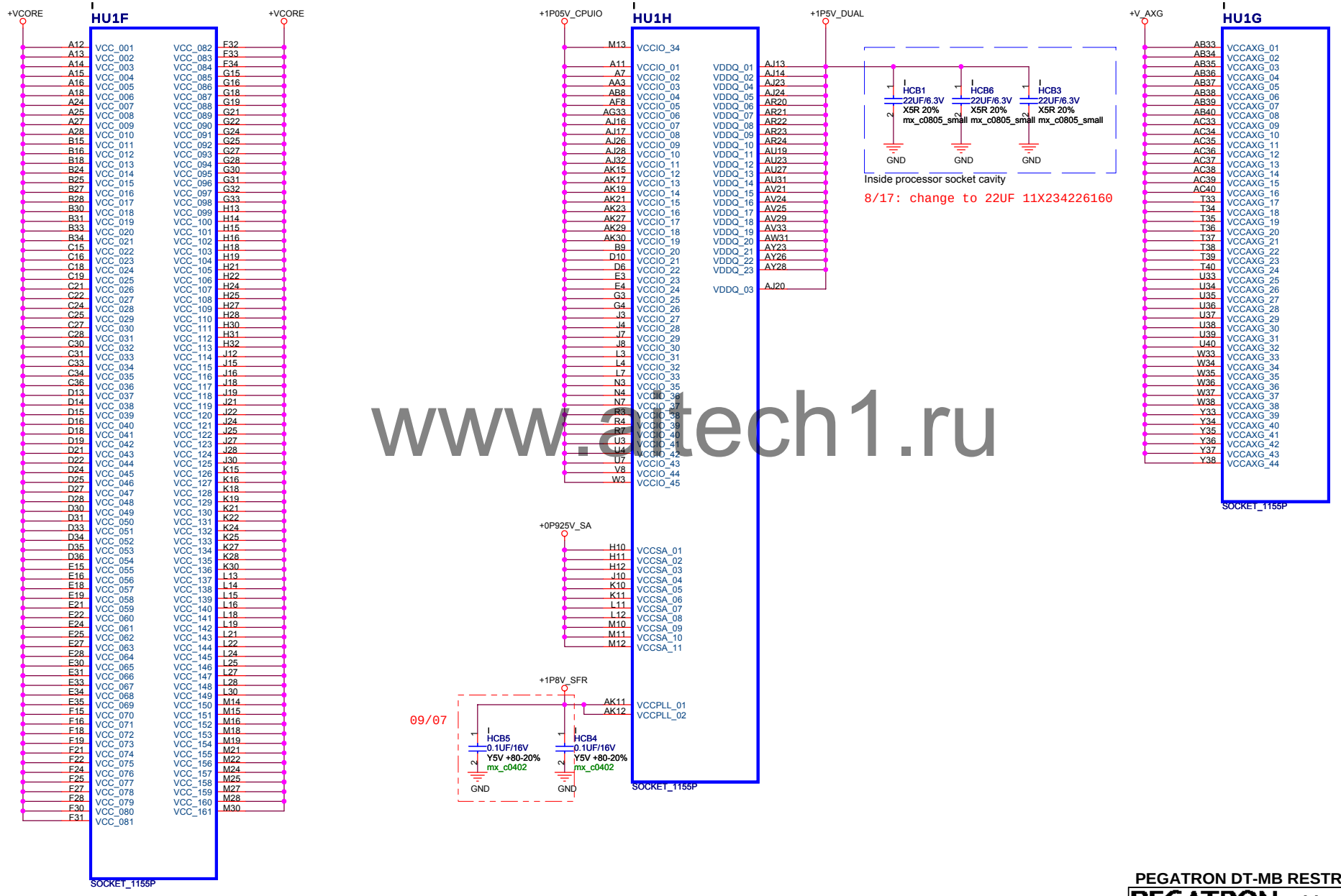
PEGATRON Title : PCIE/DMI/FDI 3-6

Pegatron Corp. Engineer: Livy_Zhu

Size	Project Name	Rev
A3	IPMSB-BE/CR	1.00

Date: Friday, September 24, 2010 Sheet 11 of 83


HU1E
MISC
SOCKET_1155P
NOTE: Place near CPU
NOTE: For VR Debug
NOTE: Place near XDP connector
Place HR23 close to NVRAM connector and minimize this stub to <100 mils with PCH and NVRAM connector
NOTE: CFG[0~15] is IPU
CFG6 CFG5 Description
1 1 X16(Default)
1 0 2X8
0 1 Reserved
0 0 X8, X4/X4
www.aitech1.ru
PEGATRON DT-MB RESTRICTED SECRET
PEGATRON Title : MISC 4-6
Pegatron Corp. Engineer: Livy_Zhu
Size A3 Project Name IPMSB-BE/CR Rev 1.00
Date: Friday, September 24, 2010 Sheet 12 of 83



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : VCC 5 - 6	
Pegatron Corp.	Engineer: Livy_Zhu	
Size: A3	Project Name: IPMSB-BE/CR	Rev: 1.00
Date: Friday, September 24, 2010	Sheet 13 of 83	

HU1I

A17	VSS_001	VSS_091	AM27
A23	VSS_002	VSS_092	AM3
A26	VSS_003	VSS_093	AM30
A29	VSS_004	VSS_094	AM36
A35	VSS_005	VSS_095	AM37
AA33	VSS_006	VSS_096	AM38
AA34	VSS_007	VSS_097	AM39
AA35	VSS_008	VSS_098	AM4
AA36	VSS_009	VSS_099	AM40
AA37	VSS_010	VSS_100	AM5
AA38	VSS_011	VSS_101	AN10
AA6	VSS_012	VSS_102	AN11
AB5	VSS_013	VSS_103	AN14
AC1	VSS_014	VSS_104	AN17
AC6	VSS_015	VSS_105	AN19
AD33	VSS_016	VSS_106	AN22
AD36	VSS_017	VSS_107	AN24
AD38	VSS_018	VSS_108	AN27
AD39	VSS_019	VSS_109	AN30
AD40	VSS_020	VSS_110	AN31
AD5	VSS_021	VSS_111	AN32
AD8	VSS_022	VSS_112	AN33
AE3	VSS_023	VSS_113	AN34
AE33	VSS_024	VSS_114	AN35
AE36	VSS_025	VSS_115	AN36
AF1	VSS_026	VSS_116	AN5
AF34	VSS_027	VSS_117	AN6
AF36	VSS_028	VSS_118	AN7
AF37	VSS_029	VSS_119	AN8
AF40	VSS_030	VSS_120	AN9
AF5	VSS_031	VSS_121	AP1
AF6	VSS_032	VSS_122	AP11
AF7	VSS_033	VSS_123	AP14
AG36	VSS_034	VSS_124	AP17
AH2	VSS_035	VSS_125	AP22
AH3	VSS_036	VSS_126	AP25
AH33	VSS_037	VSS_127	AP27
AH36	VSS_038	VSS_128	AP30
AH37	VSS_039	VSS_129	AP36
AH38	VSS_040	VSS_130	AP37
AH39	VSS_041	VSS_131	AP4
AH40	VSS_042	VSS_132	AP40
AH5	VSS_043	VSS_133	AP5
AH8	VSS_044	VSS_134	AR11
AJ12	VSS_045	VSS_135	AR14
AJ15	VSS_046	VSS_136	AR17
AJ18	VSS_047	VSS_137	AR18
AJ21	VSS_048	VSS_138	AR19
AJ25	VSS_049	VSS_139	AR27
AJ27	VSS_050	VSS_140	AR30
AJ36	VSS_051	VSS_141	AR36
AJ5	VSS_052	VSS_142	AR5
AK1	VSS_053	VSS_143	AT1
AK10	VSS_054	VSS_144	AT10
AK13	VSS_055	VSS_145	AT12
AK14	VSS_056	VSS_146	AT13
AK16	VSS_057	VSS_147	AT15
AK22	VSS_058	VSS_148	AT16
AK28	VSS_059	VSS_149	AT17
AK31	VSS_060	VSS_150	AT2
AK32	VSS_061	VSS_151	AT25
AK33	VSS_062	VSS_152	AT27
AK34	VSS_063	VSS_153	AT28
AK35	VSS_064	VSS_154	AT29
AK36	VSS_065	VSS_155	AT3
AK37	VSS_066	VSS_156	AT30
AK4	VSS_067	VSS_157	AT31
AK40	VSS_068	VSS_158	AT32
AK5	VSS_069	VSS_159	AT33
AK6	VSS_070	VSS_160	AT34
AK7	VSS_071	VSS_161	AT35
AK8	VSS_072	VSS_162	AT36
AK9	VSS_073	VSS_163	AT37
AL11	VSS_074	VSS_164	AT38
AL14	VSS_075	VSS_165	AT39
AL17	VSS_076	VSS_166	AT4
AL19	VSS_077	VSS_167	AT40
AL24	VSS_078	VSS_168	AT5
AL27	VSS_079	VSS_169	AT6
AL30	VSS_080	VSS_170	AT7
AL36	VSS_081	VSS_171	AT8
AL5	VSS_082	VSS_172	AT9
AM1	VSS_083	VSS_173	AU1
AM11	VSS_084	VSS_174	AU15
AM14	VSS_085	VSS_175	AU26
AM17	VSS_086	VSS_176	AU34
AM2	VSS_087	VSS_177	AU4
AM21	VSS_088	VSS_178	AU6
AM23	VSS_089	VSS_179	AU8
AM25	VSS_090	VSS_180	AV10
A4	VSS_NCTF_01		
AV39	VSS_NCTF_02		

GND

SOCKET_1155P

HU1J

AV11	VSS_181	VSS_271	G8
AV14	VSS_182	VSS_272	H1
AV17	VSS_183	VSS_273	H17
AV3	VSS_184	VSS_274	H2
AV35	VSS_185	VSS_275	H20
AV38	VSS_186	VSS_276	H23
AV6	VSS_187	VSS_277	H26
AW10	VSS_188	VSS_278	H29
AW11	VSS_189	VSS_279	H33
AW14	VSS_190	VSS_280	H35
AW16	VSS_191	VSS_281	H37
AW36	VSS_192	VSS_282	H39
AW6	VSS_193	VSS_283	H5
AY11	VSS_194	VSS_284	H6
AY14	VSS_195	VSS_285	H9
AY18	VSS_196	VSS_286	J11
AY35	VSS_197	VSS_287	J17
AY4	VSS_198	VSS_288	J20
AY6	VSS_199	VSS_289	J23
AY8	VSS_200	VSS_290	J26
B10	VSS_201	VSS_291	J29
B13	VSS_202	VSS_292	J32
B14	VSS_203	VSS_293	K1
B17	VSS_204	VSS_294	K12
B23	VSS_205	VSS_295	K13
B26	VSS_206	VSS_296	K14
B29	VSS_207	VSS_297	K17
B32	VSS_208	VSS_298	K2
B35	VSS_209	VSS_299	K20
B38	VSS_210	VSS_300	K23
B6	VSS_211	VSS_301	K26
C11	VSS_212	VSS_302	K29
C12	VSS_213	VSS_303	K33
C17	VSS_214	VSS_304	K35
C20	VSS_215	VSS_305	K37
C23	VSS_216	VSS_306	K39
C26	VSS_217	VSS_307	K5
C29	VSS_218	VSS_308	K6
C32	VSS_219	VSS_309	L10
C35	VSS_220	VSS_310	L17
C7	VSS_221	VSS_311	L20
C8	VSS_222	VSS_312	L23
D17	VSS_223	VSS_313	L26
D2	VSS_224	VSS_314	L29
D20	VSS_225	VSS_315	L8
D23	VSS_226	VSS_316	M1
D26	VSS_227	VSS_317	M17
D29	VSS_228	VSS_318	M2
D32	VSS_229	VSS_319	M20
D37	VSS_230	VSS_320	M23
D39	VSS_231	VSS_321	M26
D4	VSS_232	VSS_322	M29
D5	VSS_233	VSS_323	M33
D9	VSS_234	VSS_324	M35
E11	VSS_235	VSS_325	M37
E12	VSS_236	VSS_326	M39
E17	VSS_237	VSS_327	M5
E20	VSS_238	VSS_328	M6
E23	VSS_239	VSS_329	M9
E26	VSS_240	VSS_330	N8
E29	VSS_241	VSS_331	P1
E32	VSS_242	VSS_332	P2
E36	VSS_243	VSS_333	P36
E7	VSS_244	VSS_334	P38
E8	VSS_245	VSS_335	P40
F1	VSS_246	VSS_336	P5
F10	VSS_247	VSS_337	P6
F13	VSS_248	VSS_338	R33
F14	VSS_249	VSS_339	R35
F17	VSS_250	VSS_340	R37
F2	VSS_251	VSS_341	R39
F20	VSS_252	VSS_342	R8
F23	VSS_253	VSS_343	T1
F26	VSS_254	VSS_344	T5
F29	VSS_255	VSS_345	T6
F35	VSS_256	VSS_346	U8
F37	VSS_257	VSS_347	V1
F39	VSS_258	VSS_348	V2
F5	VSS_259	VSS_349	V33
F6	VSS_260	VSS_350	V34
F9	VSS_261	VSS_351	V35
G11	VSS_262	VSS_352	V36
G12	VSS_263	VSS_353	V37
G17	VSS_264	VSS_354	V38
G20	VSS_265	VSS_355	V39
G23	VSS_266	VSS_356	V40
G26	VSS_267	VSS_357	V5
G29	VSS_268	VSS_358	W6
G34	VSS_269	VSS_359	Y5
G7	VSS_270	VSS_360	Y8
AY37	VSS_NCTF_03		
B3	VSS_NCTF_04		

GND

SOCKET_1155P

HU1K

AB7	RSVD_04	FC_AH1	AH1
AD37	RSVD_05	FC_AH4	AH4
AG4	RSVD_08		
AJ29	RSVD_10	RSVD_15	AT11
AJ30	RSVD_11	RSVD_14	AP20
AJ31	RSVD_12	RSVD_13	AN20
AV34	RSVD_19	RSVD_17	AU10
AW34	RSVD_21	RSVD_22	AY10
P35			
P37	RSVD_43		
P39	RSVD_44		
R34	RSVD_45		
R36	RSVD_46		
R38	RSVD_47		
R40	RSVD_48	RSVD_07	AF4
	RSVD_49	RSVD_03	AB6
		RSVD_06	AE6
		RSVD_09	AJ11
A38	NCTF_01	RSVD_27	D38
AU40	NCTF_02	RSVD_26	C39
AW38	NCTF_03	RSVD_25	C38
C2	NCTF_04	RSVD_31	J34
D1	NCTF_05	RSVD_41	N34
		NP_NC1	1
		NP_NC2	2
		NP_NC3	3
		NP_NC4	4
		NP_NC5	5
		NP_NC6	6
		NP_NC7	7

SOCKET_1155P

NOBOM HT38 1 TP_H_NCTF_A38

SA_DIMM_VR

SB_DIMM_VR

HR42 1 2 0 mx_r0402 DIMM_DQ_VREF_A 16

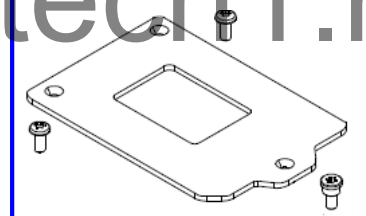
HR43 1 2 0 mx_r0402 DIMM_DQ_VREF_B 17

HC2 0.1UF/16V Y5V +80-20% mx_c0402

HC3 0.1UF/16V Y5V +80-20% mx_c0402

GND GND

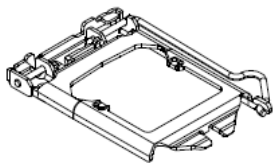
BACKPLATE1



INTEL LGA 1156P BACK PLATE,3 SCREW

PT44P11-6401

ILM1



INTEL LGA1156 SOCKET ILM

SOCKET1156_ILM

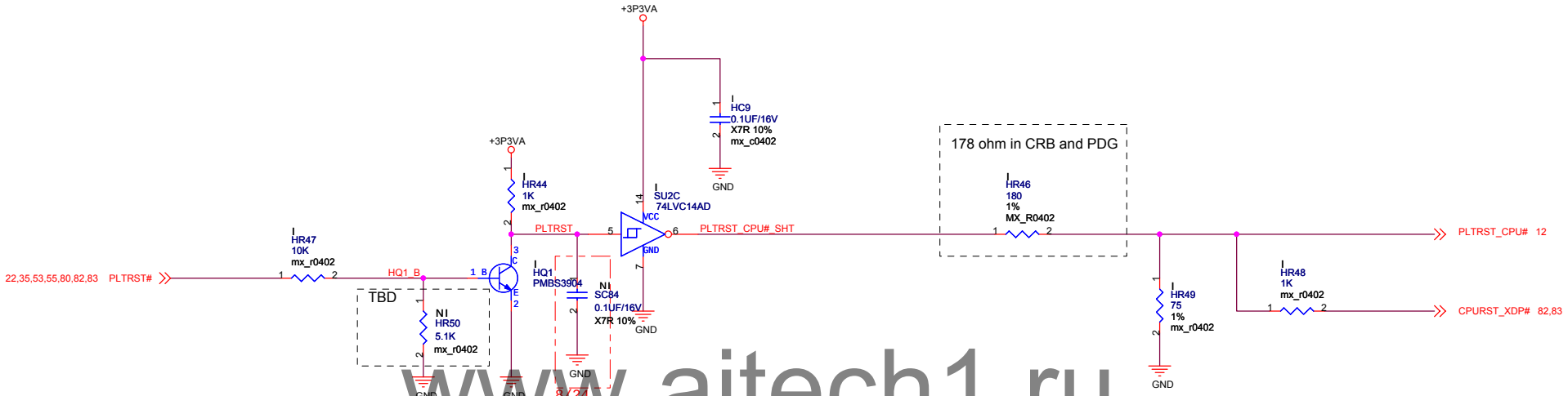
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : VSS 6 - 6

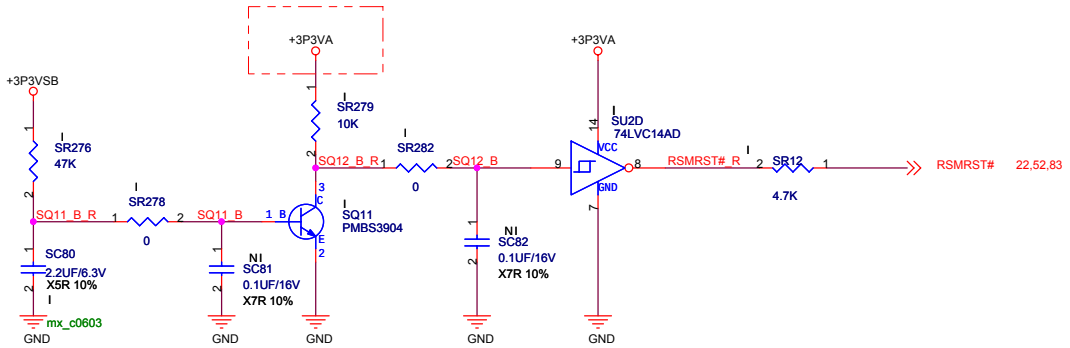
Pegatron Corp. Engineer: Livy_Zhu

Size	Project Name	Rev
A3	IPMSB-BE/CR	1.00

Date: Friday, September 24, 2010 Sheet 14 of 83

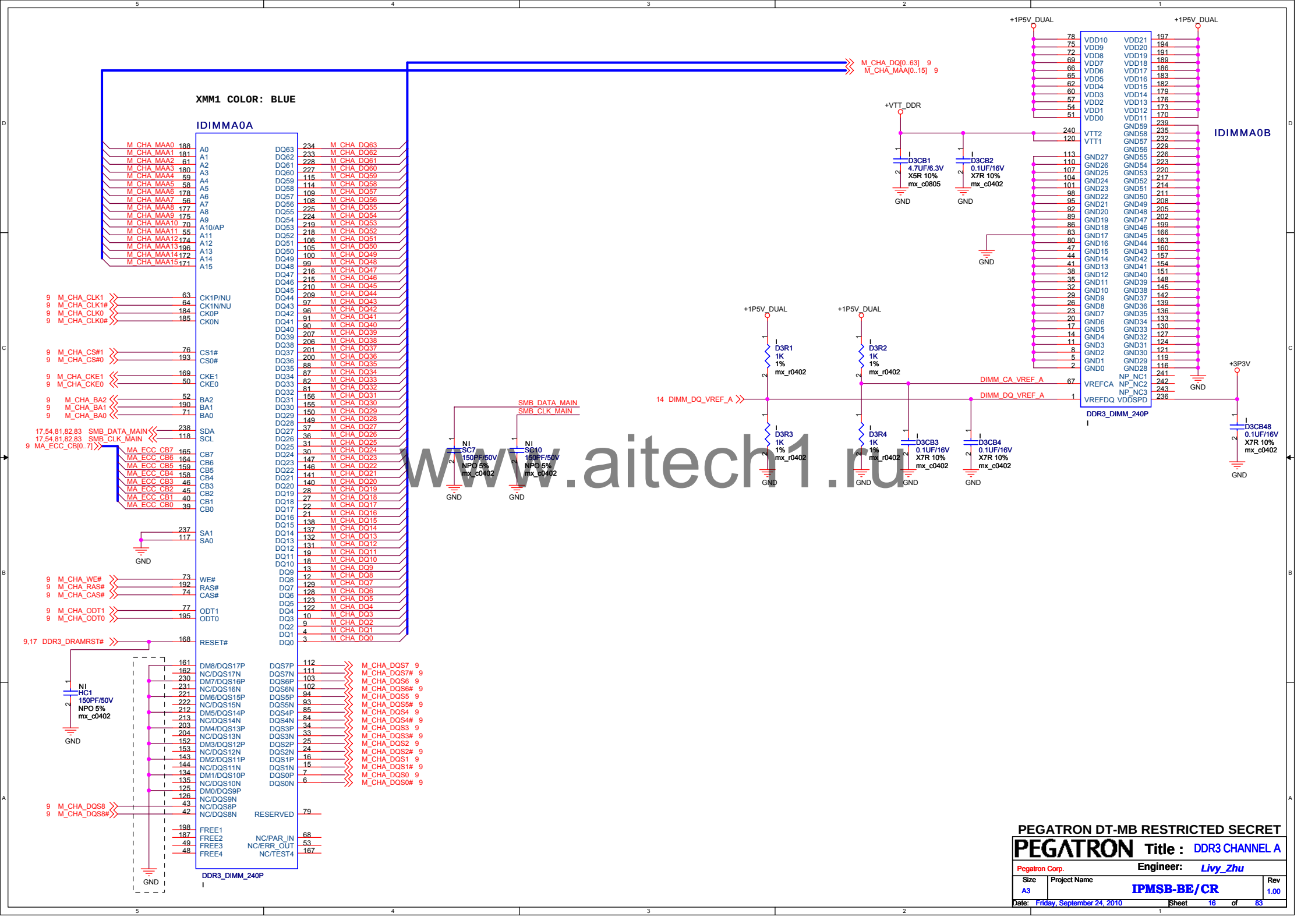


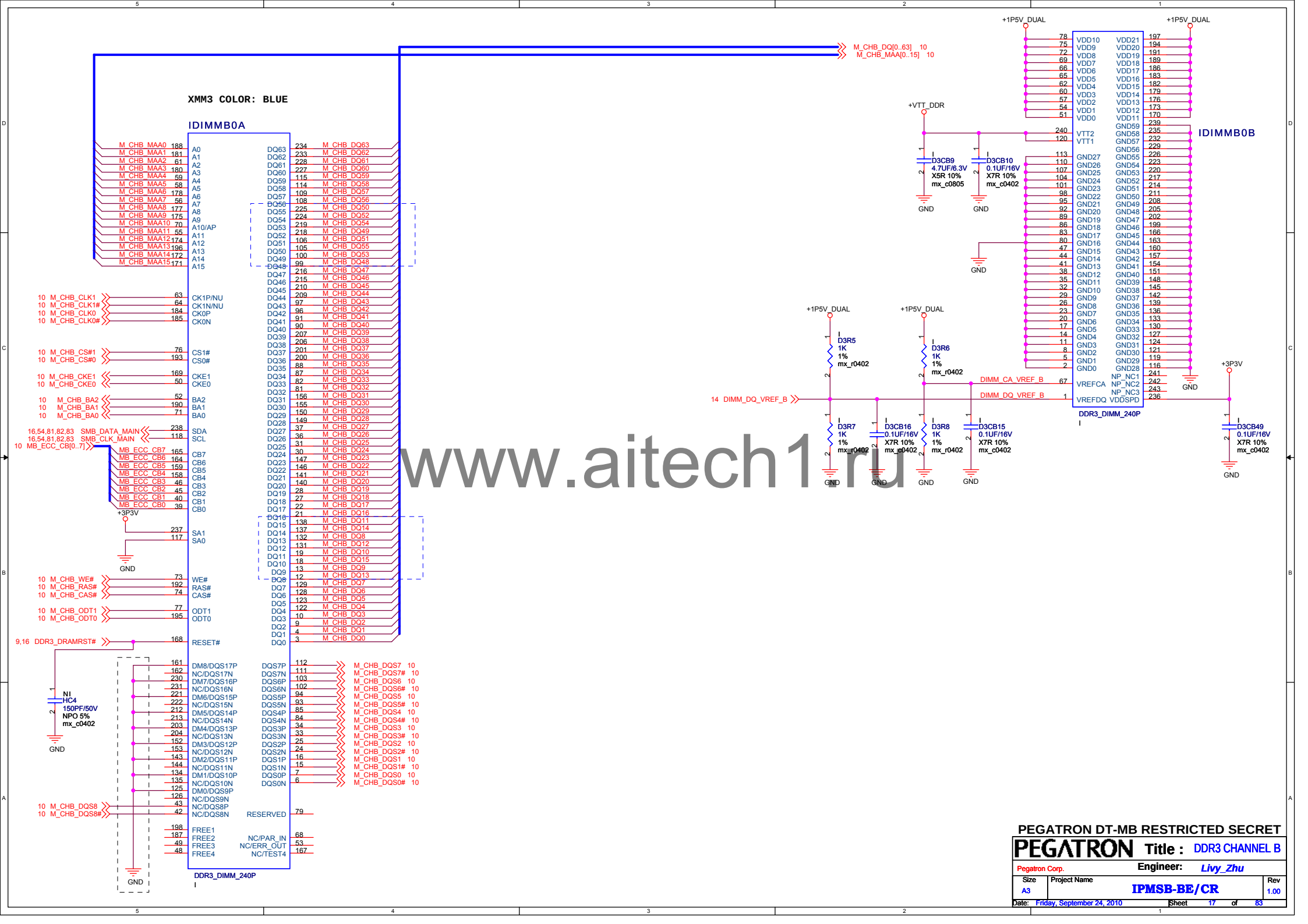
PLTRST_CPU#



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : PLTRST_CPU#	
Pegatron Corp.	Engineer: Livy_Zhu	
Size: A3	Project Name: IPMSB-BE/CR	Rev: 1.00
Date: Friday, September 24, 2010	Sheet 15 of 83	


XMM1 COLOR: BLUE
IDIMMA0A
IDIMMA0B
M_CHA_DQ[0..63] 9
M_CHA_MAA[0..15] 9
+1P5V_DUAL
+VTT_DDR
+3P3V
GND
D3CB1 4.7UF/6.3V X5R 10% mx_c0805
D3CB2 0.1UF/16V X7R 10% mx_c0402
D3R1 1K 1% mx_r0402
D3R2 1K 1% mx_r0402
D3R3 1K 1% mx_r0402
D3R4 1K 1% mx_r0402
D3CB3 0.1UF/16V X7R 10% mx_c0402
D3CB4 0.1UF/16V X7R 10% mx_c0402
D3CB48 0.1UF/16V X7R 10% mx_c0402
HC1 150PF/50V NPO 5% mx_c0402
SC7 150PF/50V NPO 5% mx_c0402
SC10 150PF/50V NPO 5% mx_c0402
DIMM_CA_VREF_A
DIMM_DQ_VREF_A
SMB_DATA_MAIN
SMB_CLK_MAIN
DDR3_DIMM_240P
DDR3_DRAMRST#
MA_ECC_CB[0..7]
www.aitech1.ru
PEGATRON DT-MB RESTRICTED SECRET
PEGATRON
Title : DDR3 CHANNEL A
Pegatron Corp.
Engineer: Livy_Zhu
Size A3
Project Name IPMSB-BE/CR
Rev 1.00
Date: Friday, September 24, 2010
Sheet 16 of 83



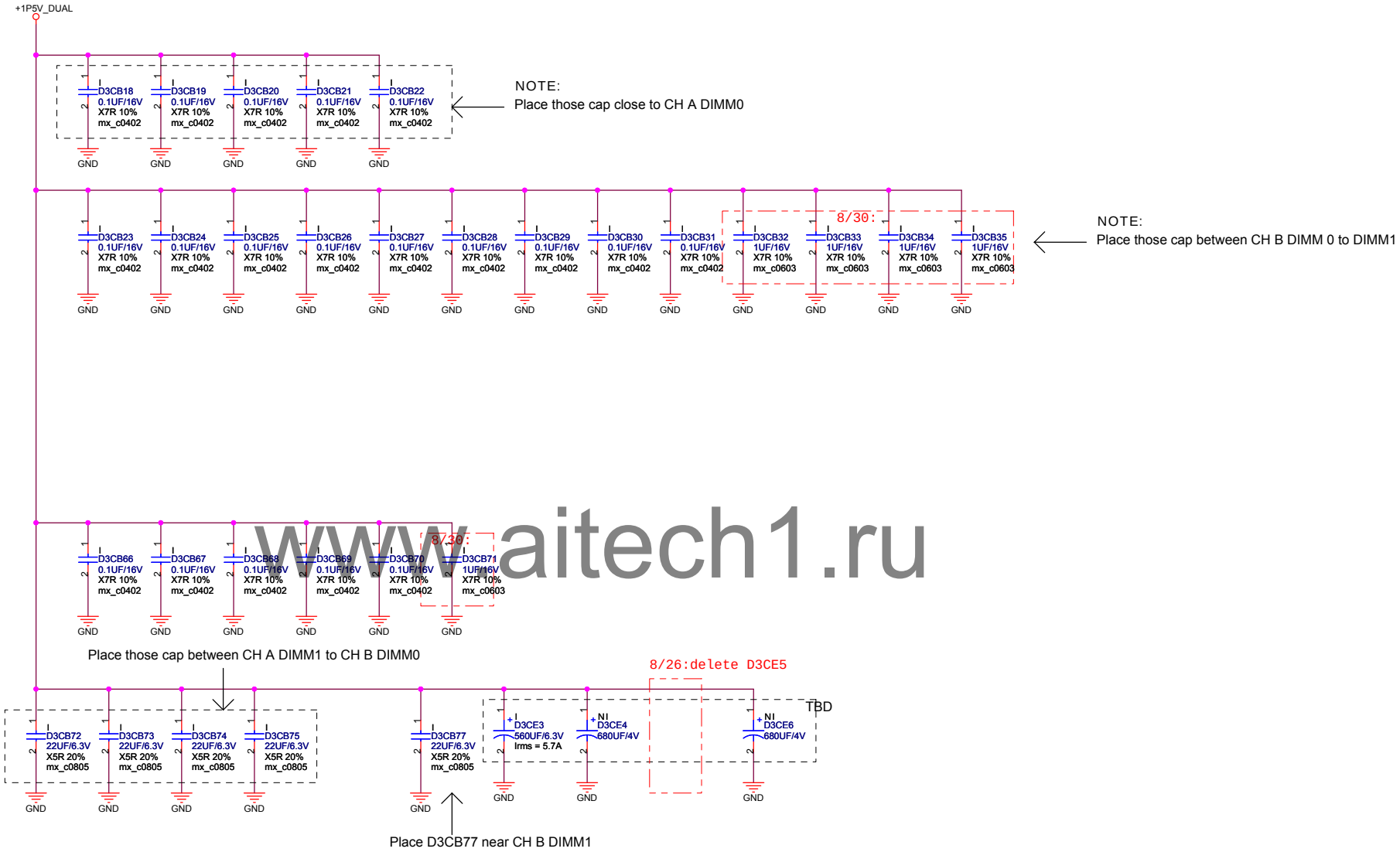
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : DDR3 CHANNEL B

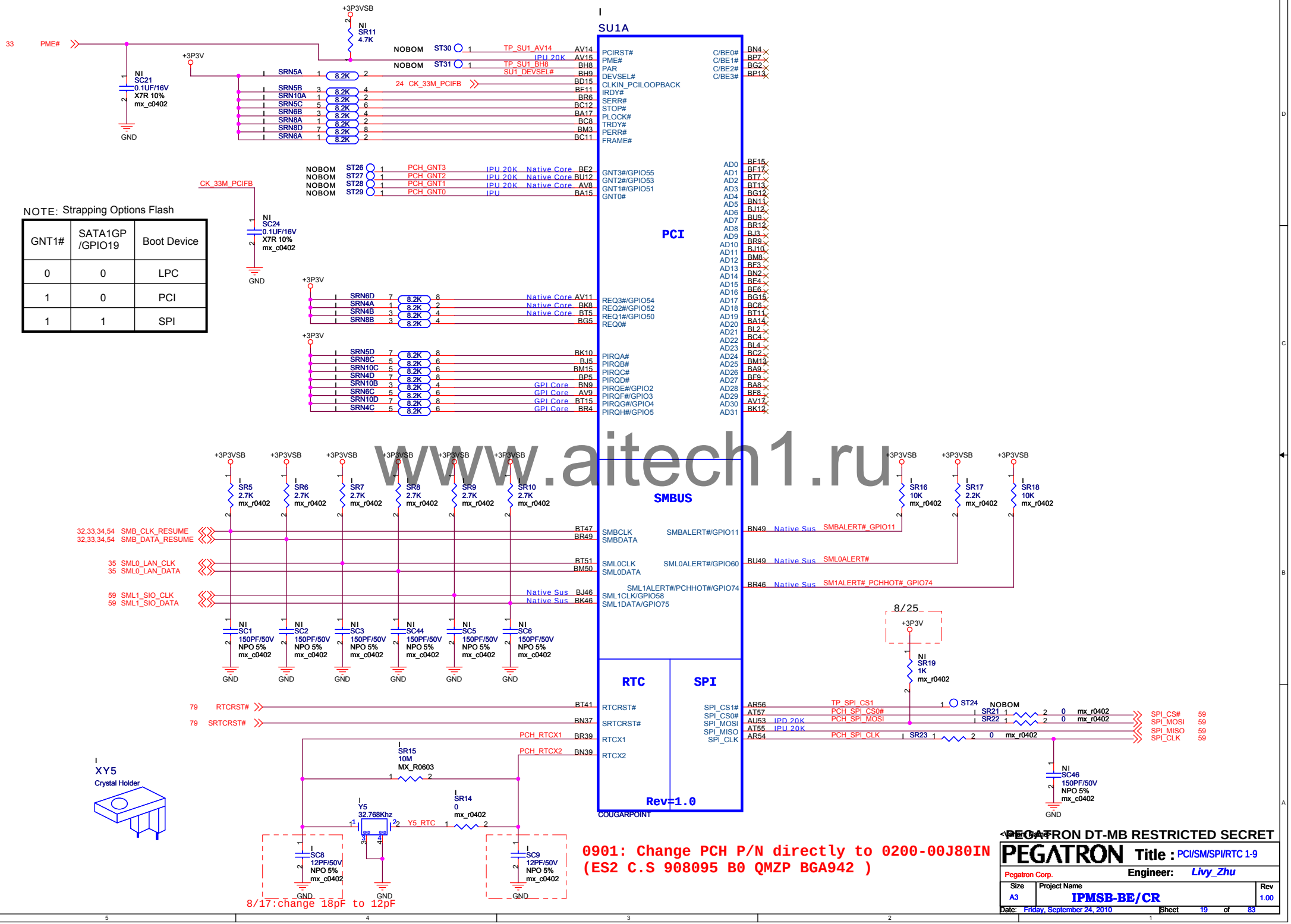
Pegatron Corp. Engineer: Livy_Zhu

Size	Project Name	Rev
A3	IPMSB-BE/CR	1.00

Date: Friday, September 24, 2010 Sheet 17 of 83



PEGATRON	Title : DDR3 TERMINATION A&B	
Pegatron Corp.	Engineer: Livy_Zhu	
Size: A3	Project Name: IPMSB-BE/CR	Rev: 1.00
Date: Friday, September 24, 2010	Sheet 18 of 83	



NOTE: Strapping Options Flash

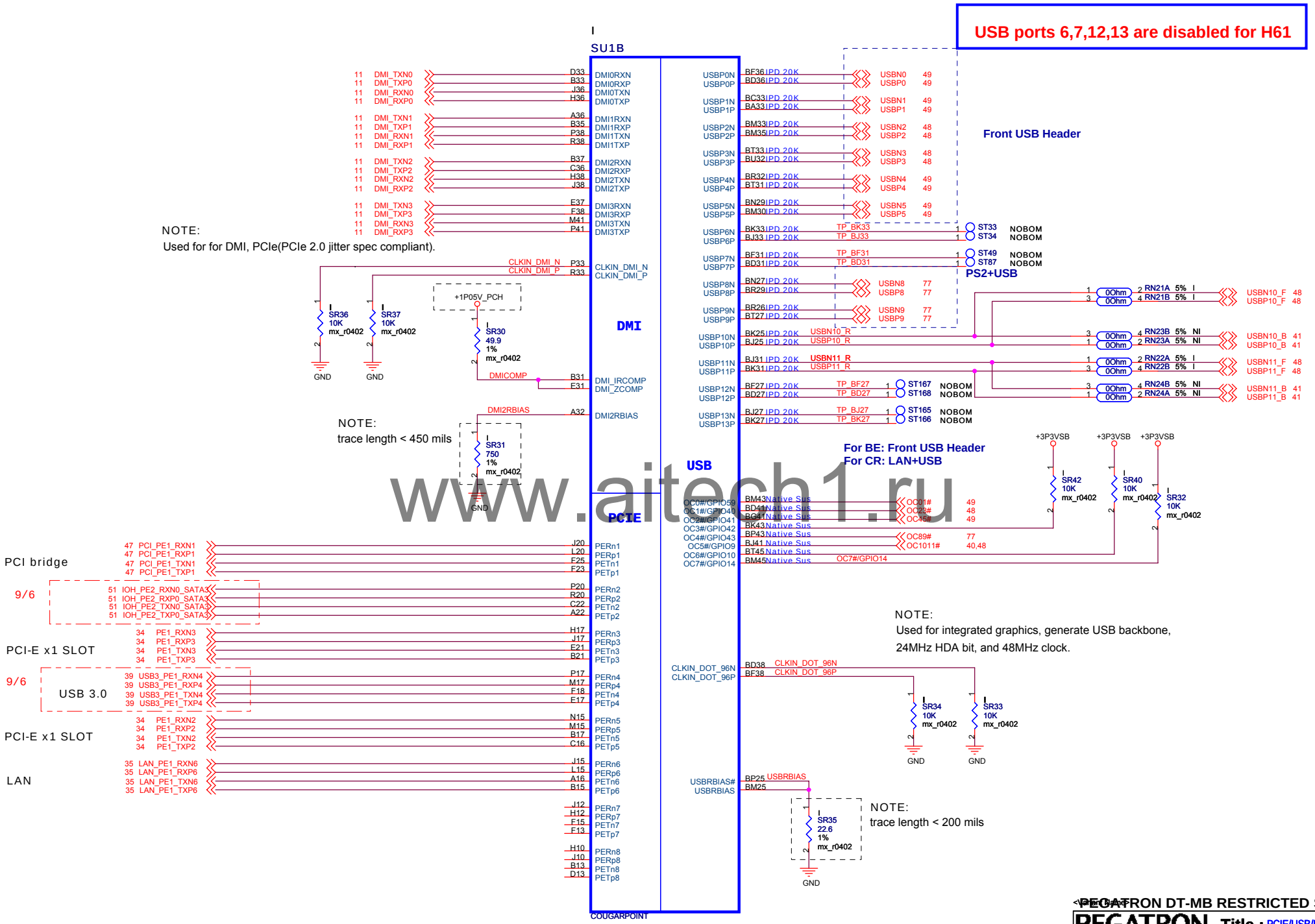
GNT1#	SATA1GP /GPIO19	Boot Device
0	0	LPC
1	0	PCI
1	1	SPI

PEGATRON Title : PCI/SM/SPI/RTC 1-9

Pegatron Corp. Engineer: Livy_Zhu

Size	Project Name	Rev
A3	IPMSB-BE/CR	1.00

Date: Friday, September 24, 2010 Sheet 19 of 83



PEGATRON	Title : PCIE/USB/DMI 2-9	
Pegatron Corp.	Engineer: Livy_Zhu	
Size: A3	Project Name: IPMSB-BE/CR	Rev: 1.00
Date: Friday, September 24, 2010	Sheet 20 of 83	

NOTE:

SR40	SR41	Description
I	NI	iAMT
NI	I	non iAMT

SU1C

CLINK
FAN
GPIO
HOST
COUGARPOINT

NOBOM ST21 1 TP_CL_CLK1 IPU 32/ IPD 100 BA50
NOBOM ST22 1 TP_CL_DATA1 IPU 32/ IPD 100 BE50
NOBOM ST23 1 TP_CL_RST1# BF49
CL_CLK1
CL_DATA1
CL_RST1#

22,52 PWROK — SR41 0 mx_r0402 — PCH_MEPWROK BC46
APWROK
NI SC30 100PF/50V NPO 5% mx_c0402 GND

NOBOM ST38 1 TP_SU1_PWM0 BN21
NOBOM ST39 1 TP_SU1_PWM1 BT21
NOBOM ST25 1 TP_SU1_PWM2 BM20
NOBOM ST44 1 TP_SU1_PWM3 BN19
PWM0
PWM1
PWM2
PWM3

+3P3V: SR50 10K mx_r0402, SR49 10K mx_r0402, SR52 10K mx_r0402, SR47 10K mx_r0402, SR51 10K mx_r0402

GPI Core IPU 20K BT17 — TACH0/GPIO17
CATERR# GPI — GPI Core IPU 20K BR19 — TACH1/GPIO1
39 USB3_SMI# — GPI Core IPU 20K BA22 — TACH2/GPIO6
52 SIO_SMI# — GPI Core IPU 20K BR16 — TACH3/GPIO7
GPI Core IPU 20K BU16 — TACH4/GPIO68
GPI Core IPU 20K BM18 — TACH5/GPIO69
57 R_FAN_INITIAL — Native Core IPU 20K BN17 — TACH6/GPIO70
56 F_FAN_INITIAL — Native Core IPU 20K BP15 — TACH7/GPIO71

SST IPD 10K BC43
NI SC31 220PF/50V X7R 10% mx_c0402 GND

+3P3V: NI SR55 10K mx_r0402, NI SR64 10K mx_r0402, NI SR65 10K mx_r0402

80 BIOS_CONF1 — GPI Core BA53 — SCLOCK/GPIO22
Board_ID_0 — GPI Core BE54 — SLOAD/GPIO38
Board_ID_1 — GPI Core BF55 — SDATAOUT0/GPIO39
Board_ID_2 — GPI Core AW53 — SDATAOUT1/GPIO48

+3P3V: SR56 10K mx_r0402, SR57 10K mx_r0402, SR58 10K mx_r0402

CLKIN_SATA_N AF55
CLKIN_SATA_P AG56
SR38 10K mx_r0402, SR39 10K mx_r0402
CLKIN_SATA_N
CLKIN_SATA_P

AY20 NC_1

SATA0RXN AC56 — SATA_RXN0 50
SATA0RXP AB55 — SATA_RXP0 50
SATA0TXN AE46 — SATA_TXN0 50
SATA0TXP AE44 — SATA_TXP0 50
SATA1RXN AA53 — SATA_RXN1 50
SATA1RXP AA56 — SATA_RXP1 50
SATA1TXN AG49 — SATA_TXN1 50
SATA1TXP AG47 — SATA_TXP1 50
SATA2RXN AL50
SATA2RXP AL49
SATA2TXN AL56
SATA2TXP AL53
SATA3RXN AN46
SATA3RXP AN44
SATA3TXN AN56
SATA3TXP AM55
SATA4RXN AN49 — SATA_RXN4 50
SATA4RXP AN50 — SATA_RXP4 50
SATA4TXN AT50 — SATA_TXN4 50
SATA4TXP AT49 — SATA_TXP4 50
SATA5RXN AT46 — SATA_RXN5 50
SATA5RXP AT44 — SATA_RXP5 50
SATA5TXN AV50 — SATA_TXN5 50
SATA5TXP AV49 — SATA_TXP5 50

+1P05V_CPUIO: SR83 51 mx_r0402, NI HC10 0.1UF/16V X7R 10% mx_c0402 GND
CATERR# BASE — PQ28 PMBS3904 — CATERR# GPI
12,79 CATERR#

+3P3V: SR46 10K mx_r0402

SATA0GP/GPIO21 BC54 GPI Core — Board_ID_3
SATA1GP/GPIO19 AY52 GPI Core IPU 20K — SATA1GP_GPIO19 — SR61 10K mx_r0402
SATA2GP/GPIO36 BB55 GPI Core IPD 20K — SATA2GP_GPIO36 — SR62 10K mx_r0402
SATA3GP/GPIO37 BG53 GPI Core IPD 20K — SATA3GP_GPIO37 — SR63 10K mx_r0402
SATA4GP/GPIO16 AU56 GPI Core — FAB_ID_0
SATA5GP/GPIO49 BA56 GPI Core — FAB_ID_1

EDS 1.0 SATA2GP/SATA3GP should not be pulled high when strap is sampled.

+3P3V: IN SR60 10K mx_r0402, IN SR45 10K mx_r0402, IN SR48 10K mx_r0402
GND
+3P3V: SR82 10K mx_r0402, SR88 10K mx_r0402, SR85 10K mx_r0402

SATAICOMPI AJ55
SATAICOMPO AJ53 — SATAICOMP — NOTE: trace length < 500 mils — +1P05V_PCH — SR66 37.4 1% mx_r0402
SATA3COMPI AE54
SATA3RCOMPO AE52 — SATA3COMP — NOTE: trace length < 500 mils — +1P05V_PCH — SR67 49.9 1% mx_r0402
+3P3V — SR68 10K mx_r0402
SATALED# BF57 — HD_LED# 58
TP16 AE50
SATA3RBIAS AC52 — SATA3RBIAS — NOTE: trace length < 450 mils — SR70 750 1% mx_r0402 GND

Fab.ID

	GPIO49	GPIO16
1.00	0	0
1.01	0	1

Board ID

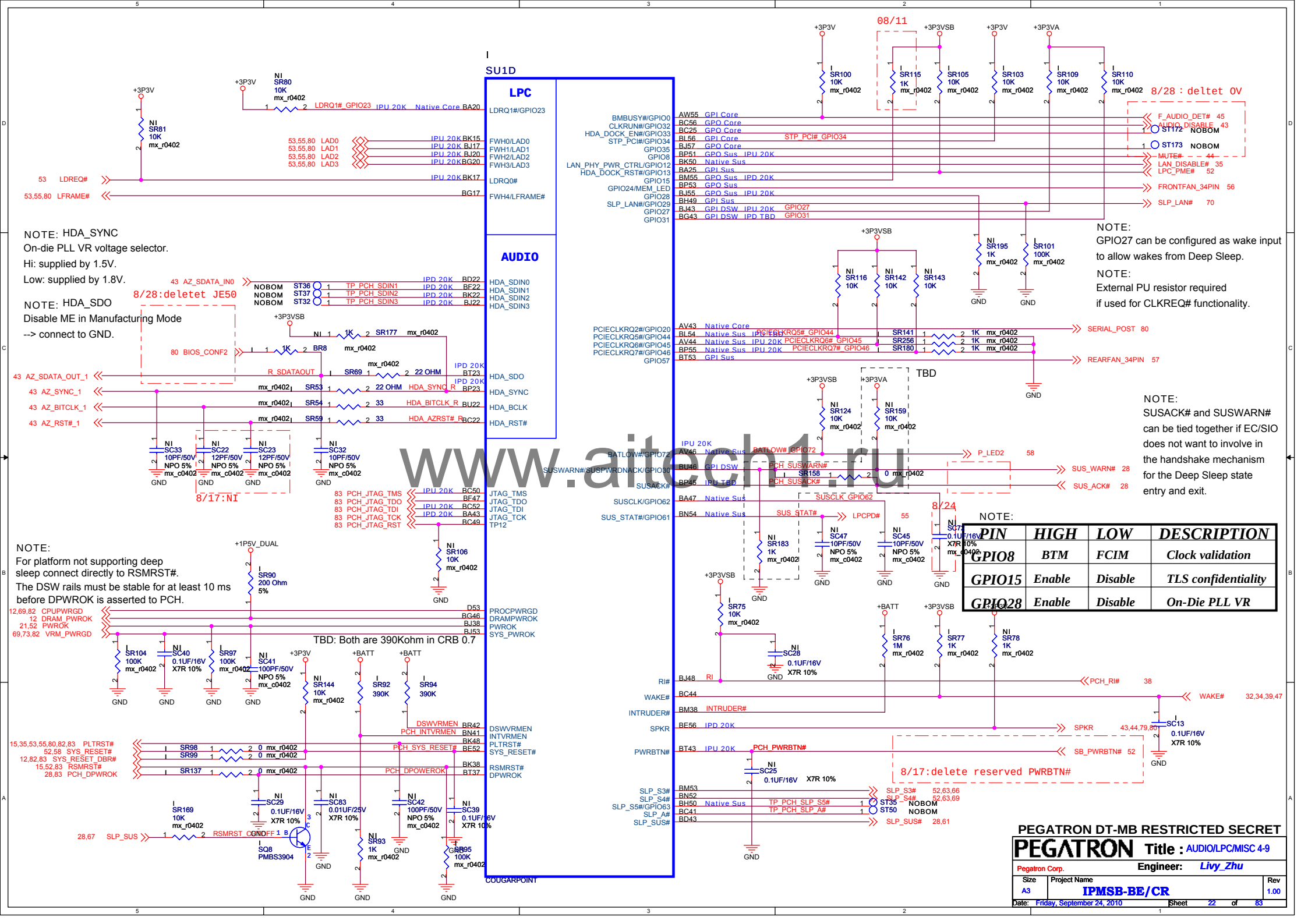
	GPIO21	GPIO48	GPIO39	GPIO38
BE	0	0	0	0
CR	0	0	0	1

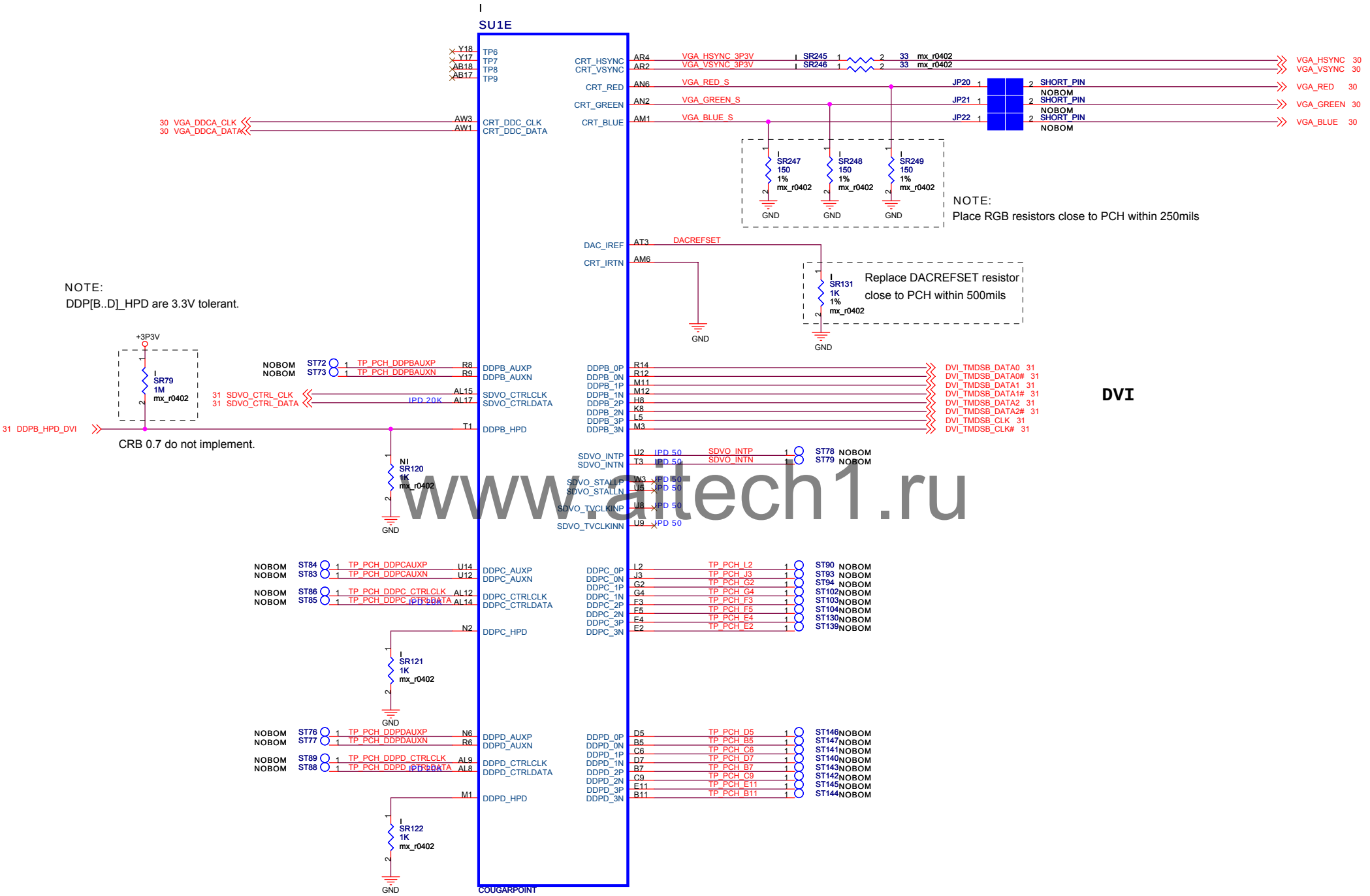
+1P05V_CPUIO: NI HR19 51 mx_r0402
+3P3V: NI SR113 10K mx_r0402, SR73 10K mx_r0402, NI SR114 10K mx_r0402
SIOD5 BAT54AW
NI mx_r0402 SR43 — TPM_SERIRQ 55

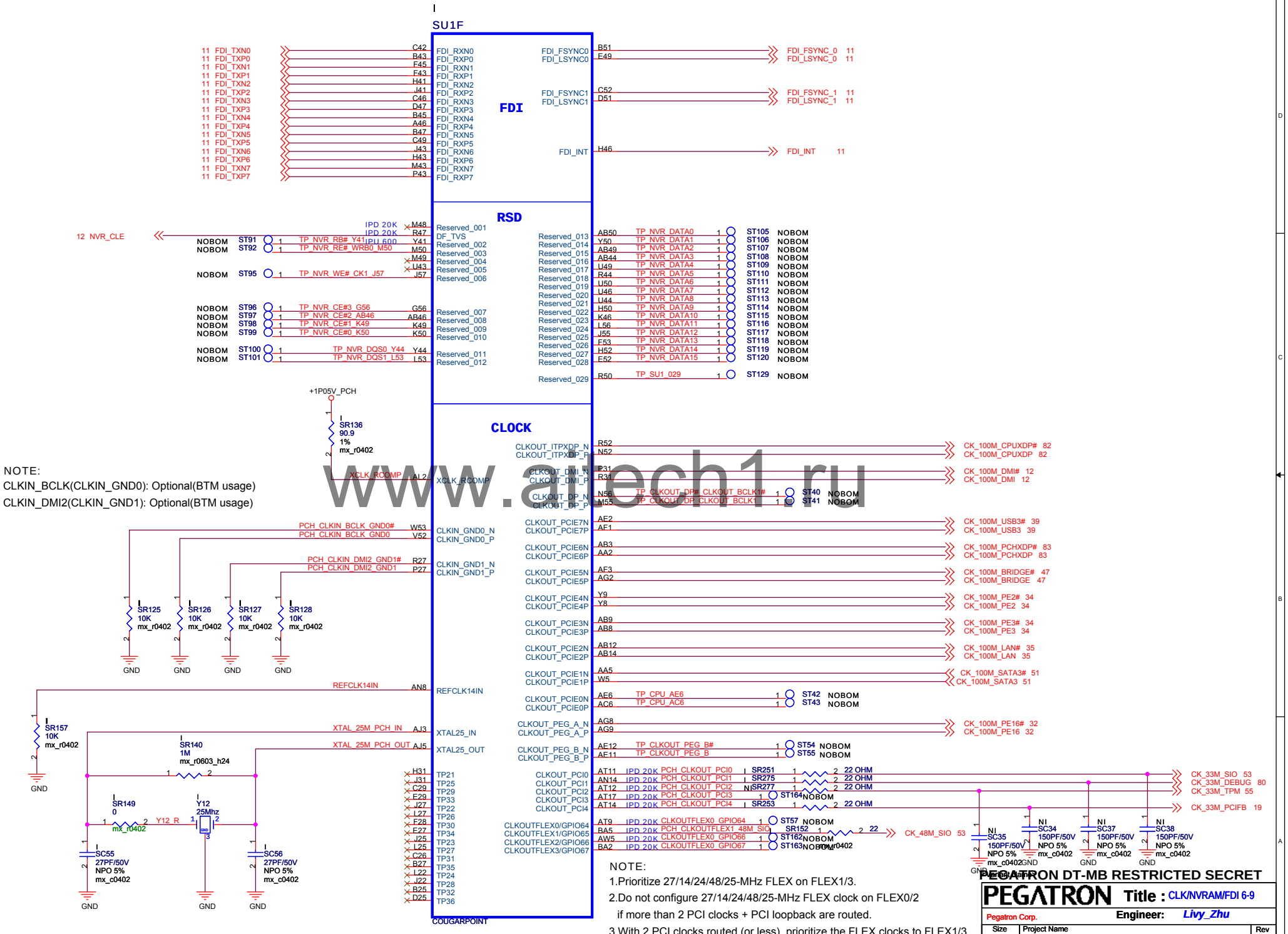
BB57 — A20GATE 53
A20GATE
BN56 IPU 20K — INIT3_3V#
INIT3_3V#
BG56 — RCIN#
AV52 — SERIRQ — mx_r0402 SR44 — RST_KB# 53, SERIRQ 53
E56 — THRMTRIP# — H_THMTRIP# 12
H48 IPD 0.35K — PECI — PECI_PCH 12
F55 — PMSYNCH — PM_SYNC 12

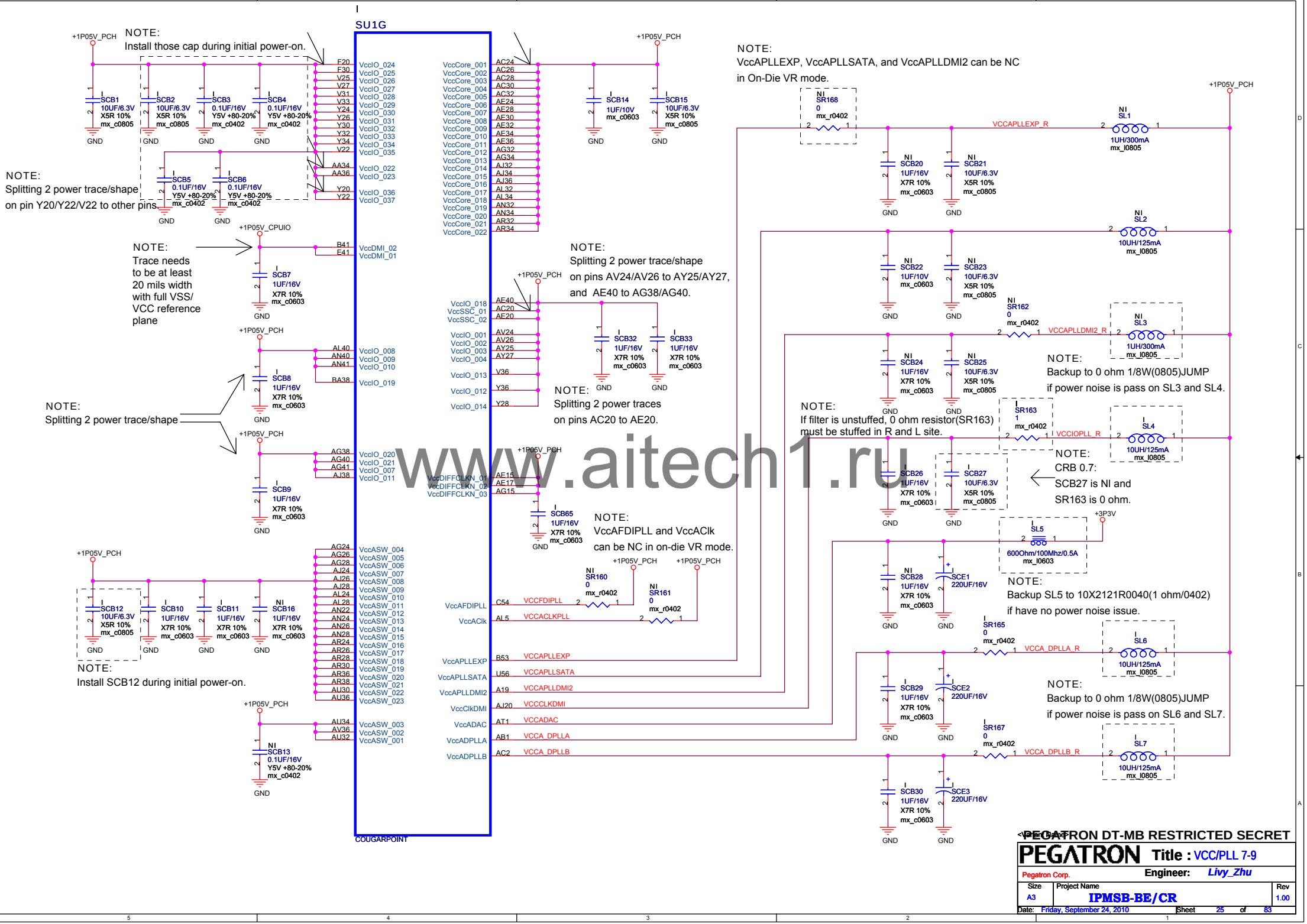
NI SR74 1K mx_r0402 GND
NI HC8 0.1UF/16V X7R 10% mx_c0402 GND
NI O2C23 0.1UF/16V mx_c0402 GND

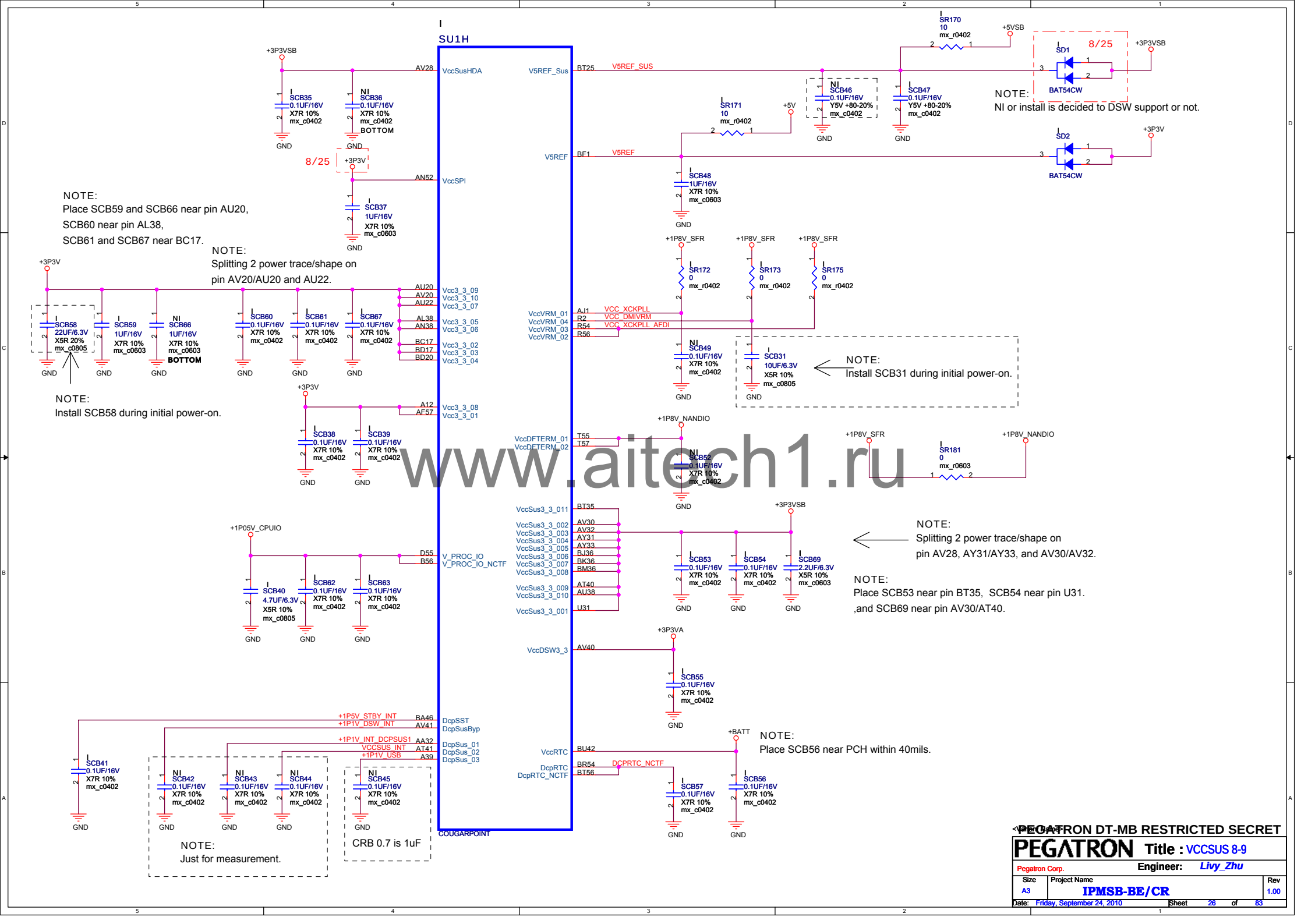
PEGATRON Title : SATA/HOST/FAN 3-9
Pegatron Corp. Engineer: Livy_Zhu
Size A3 | Project Name IPMSB-BE/CR | Rev 1.00
Date: Friday, September 24, 2010 | Sheet 21 of 83











PEGATRON Title : VCCSUS 8-9

Pegatron Corp. Engineer: Livy_Zhu

Size	Project Name	Rev
A3	IPMSB-BE/CR	1.00

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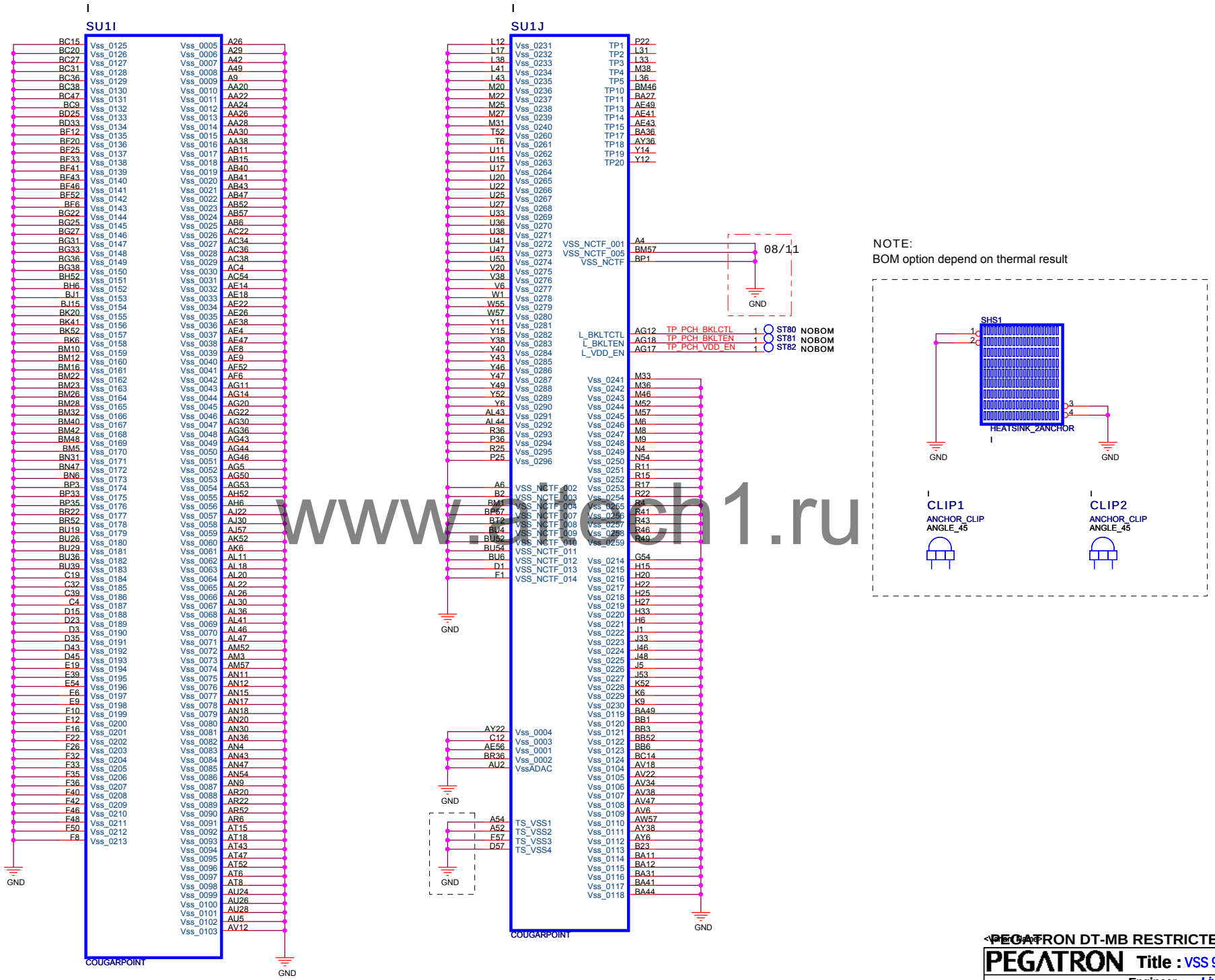

PEGATRON Title : VSS 9-9

Pegatron Corp. Engineer: Livy_Zhu

Size	Project Name	Rev
A3	IPMSB-BE/CR	1.00

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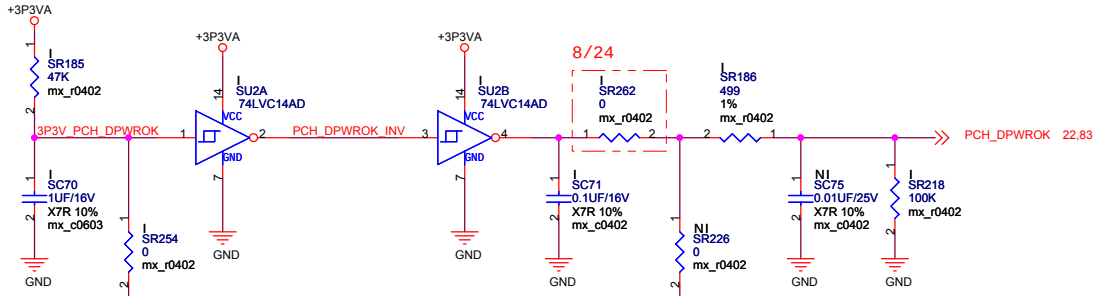
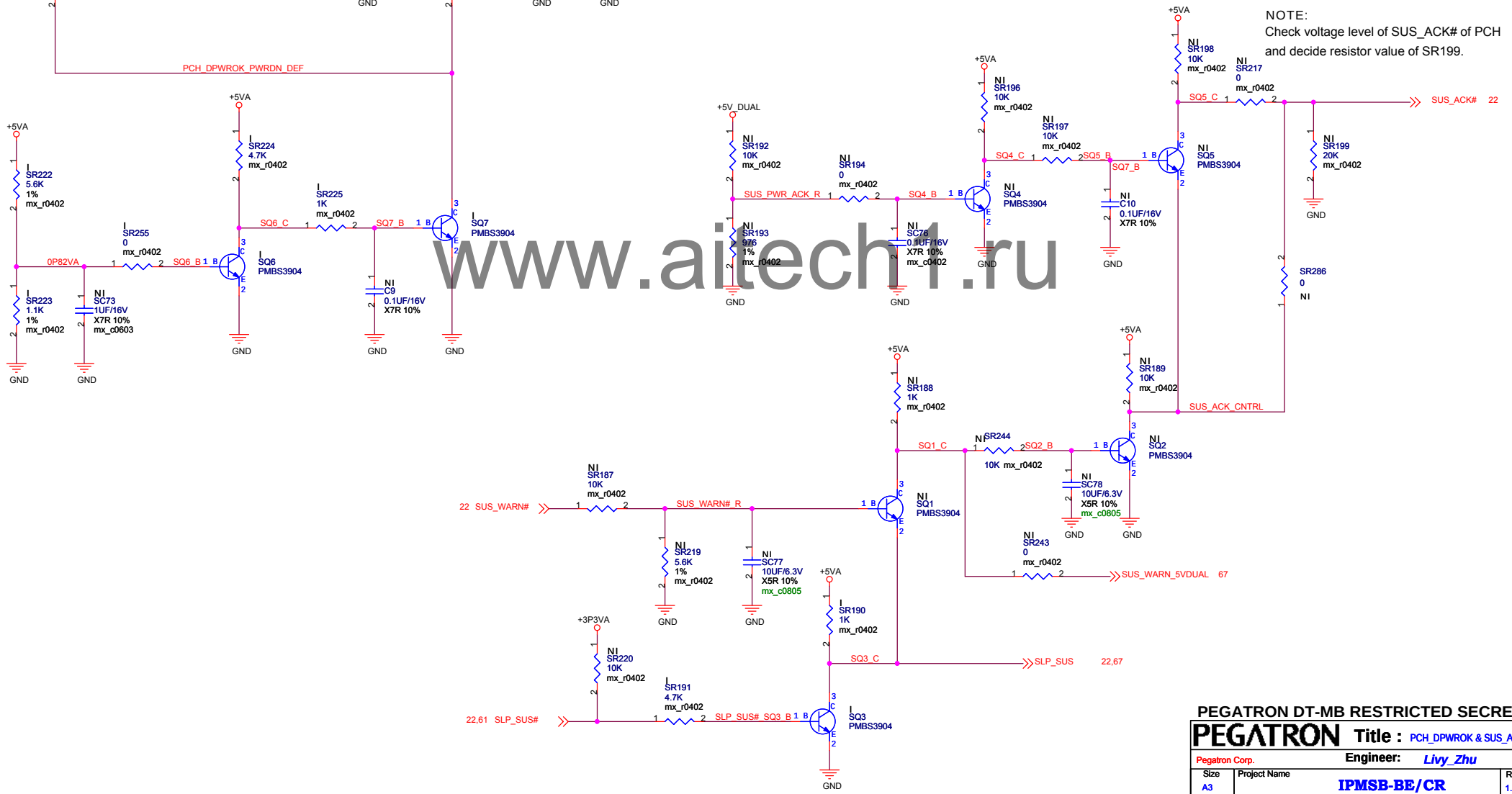
PCH_DPWROK



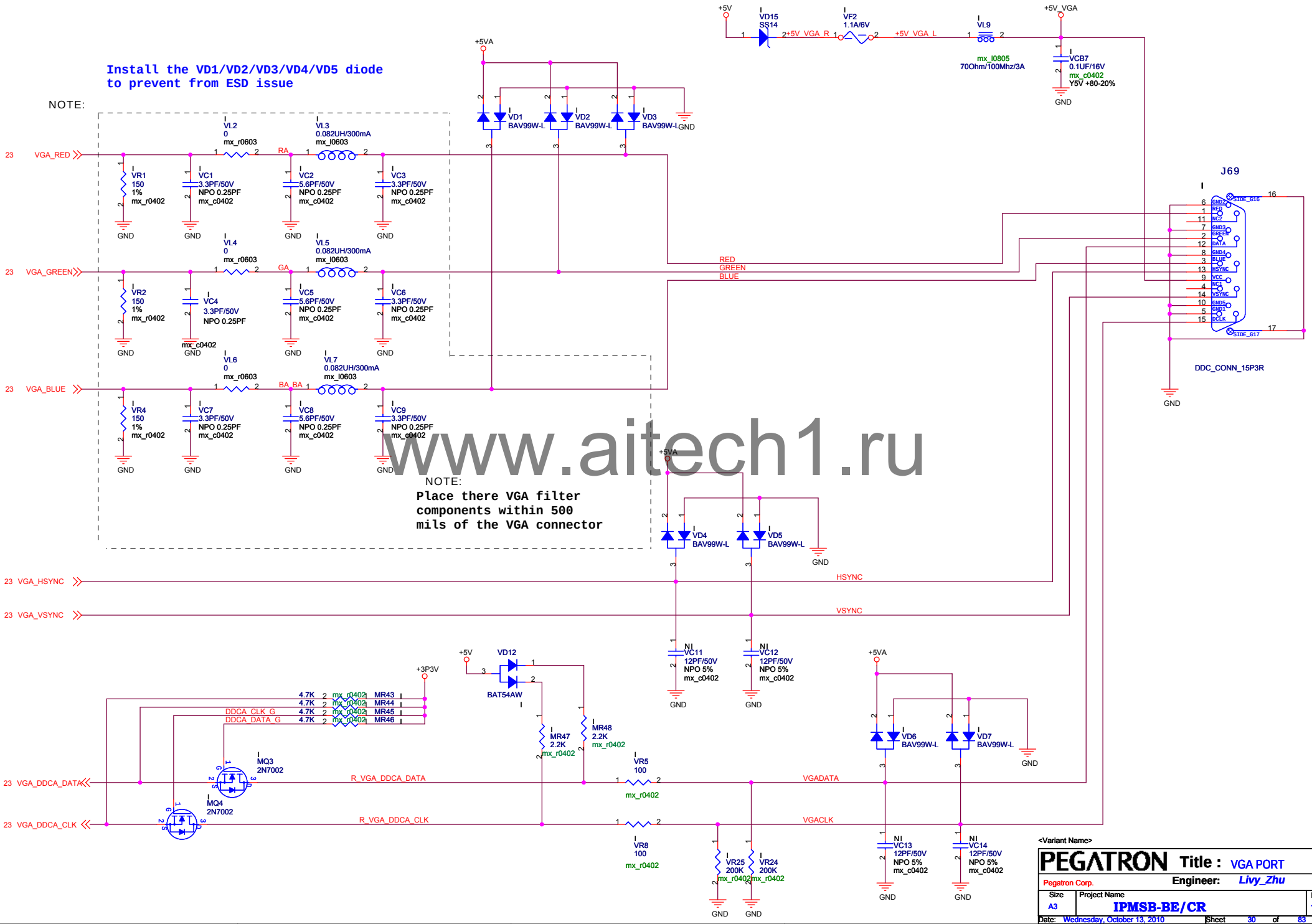
SUS_ACK#

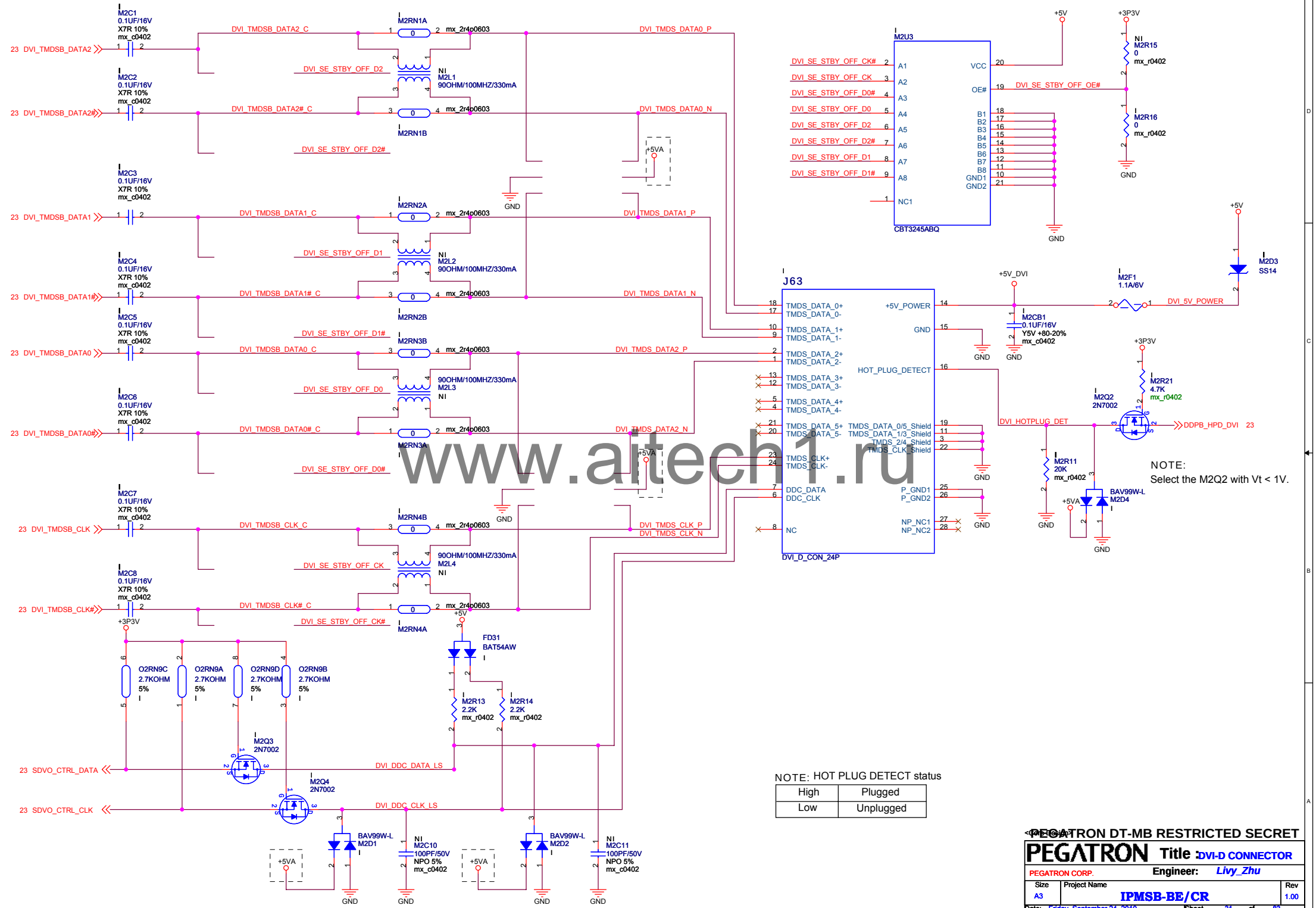
NOTE:
Check voltage level of SUS_ACK# of PCH and decide resistor value of SR199.



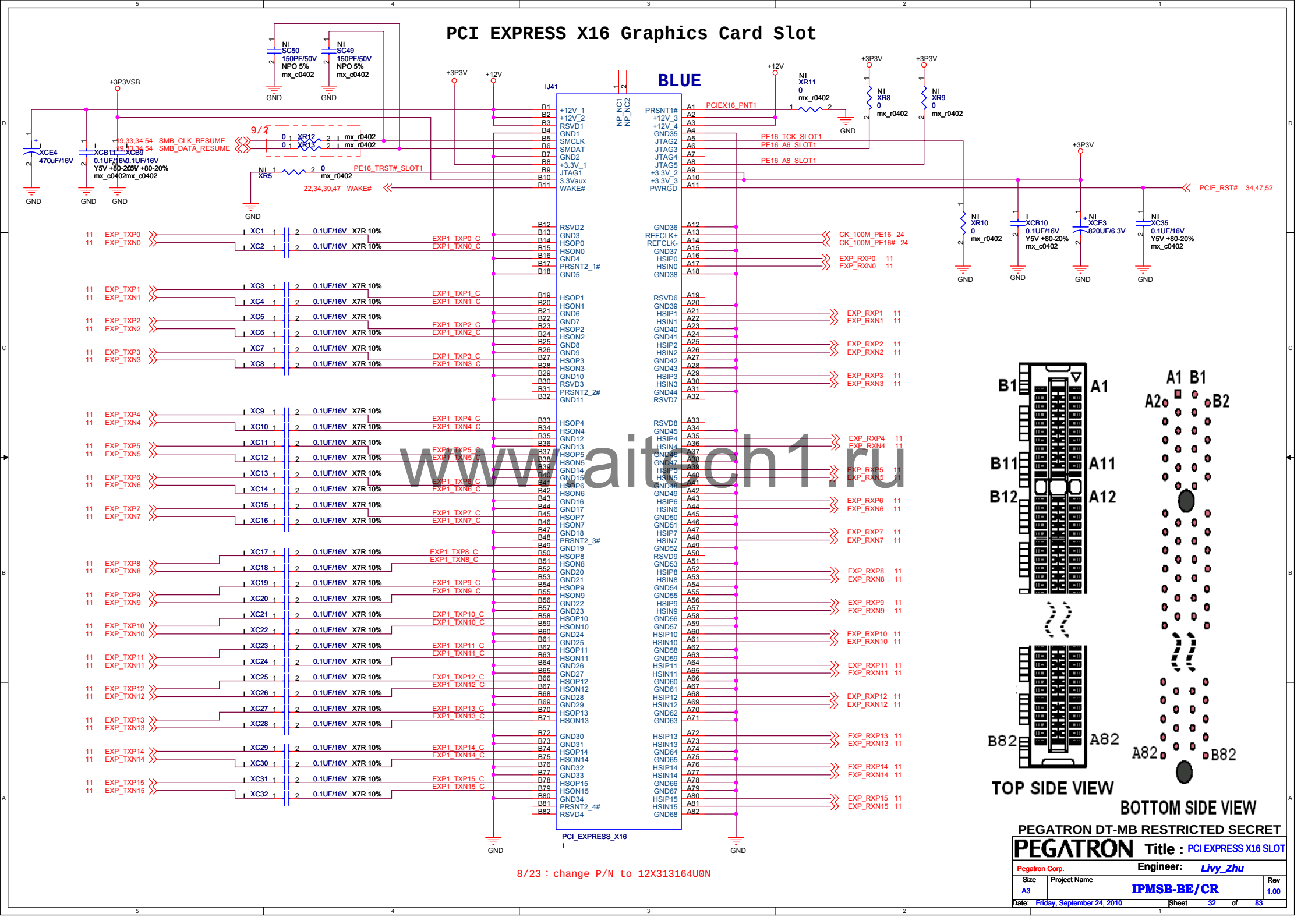
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : PCH_DPWROK & SUS_ACK#	
Pegatron Corp.	Engineer: Livy_Zhu	
Size: A3	Project Name: IPMSB-BE/CR	Rev: 1.00
Date: Friday, September 24, 2010	Sheet 28 of 83	





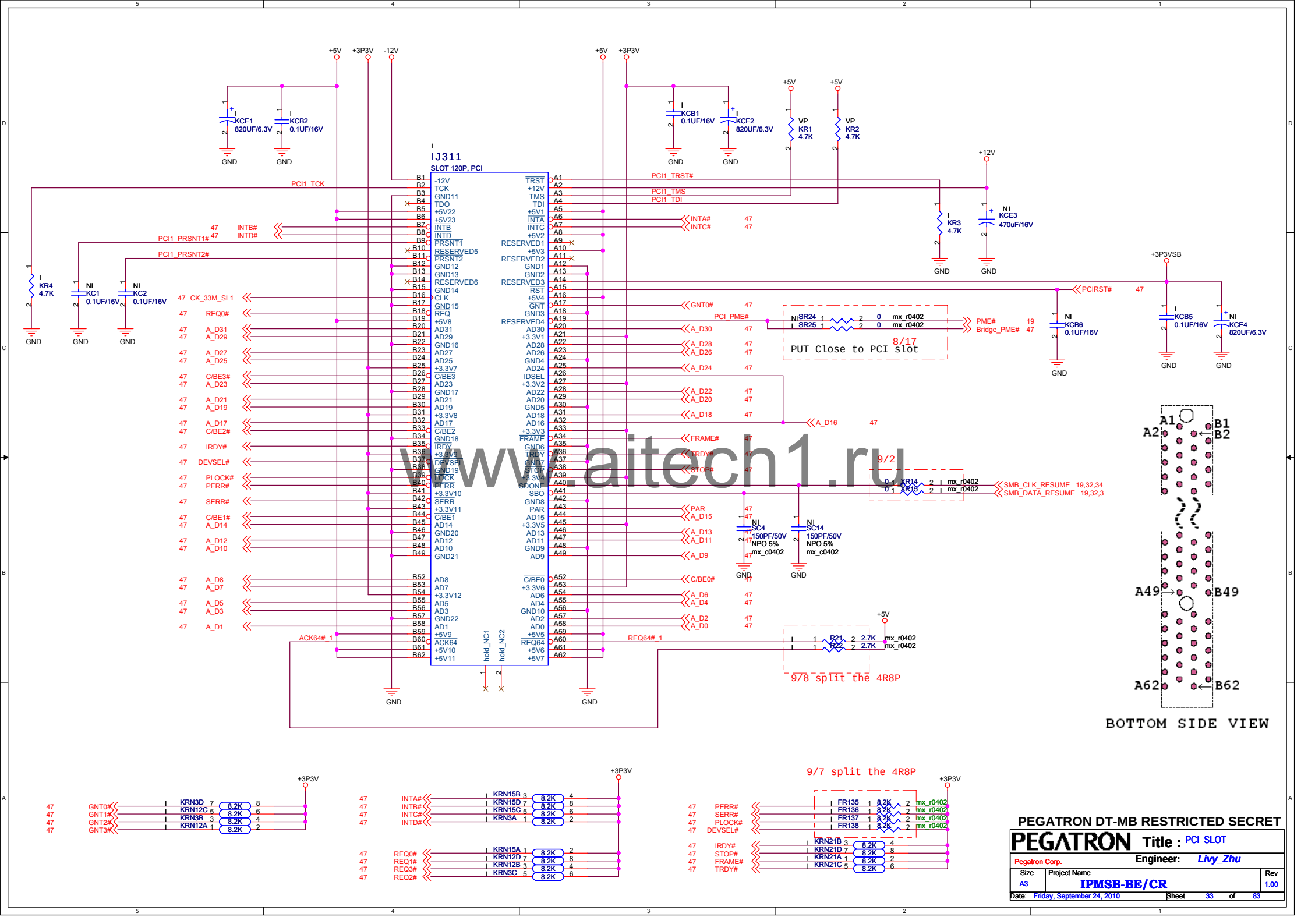
PCI EXPRESS X16 Graphics Card Slot

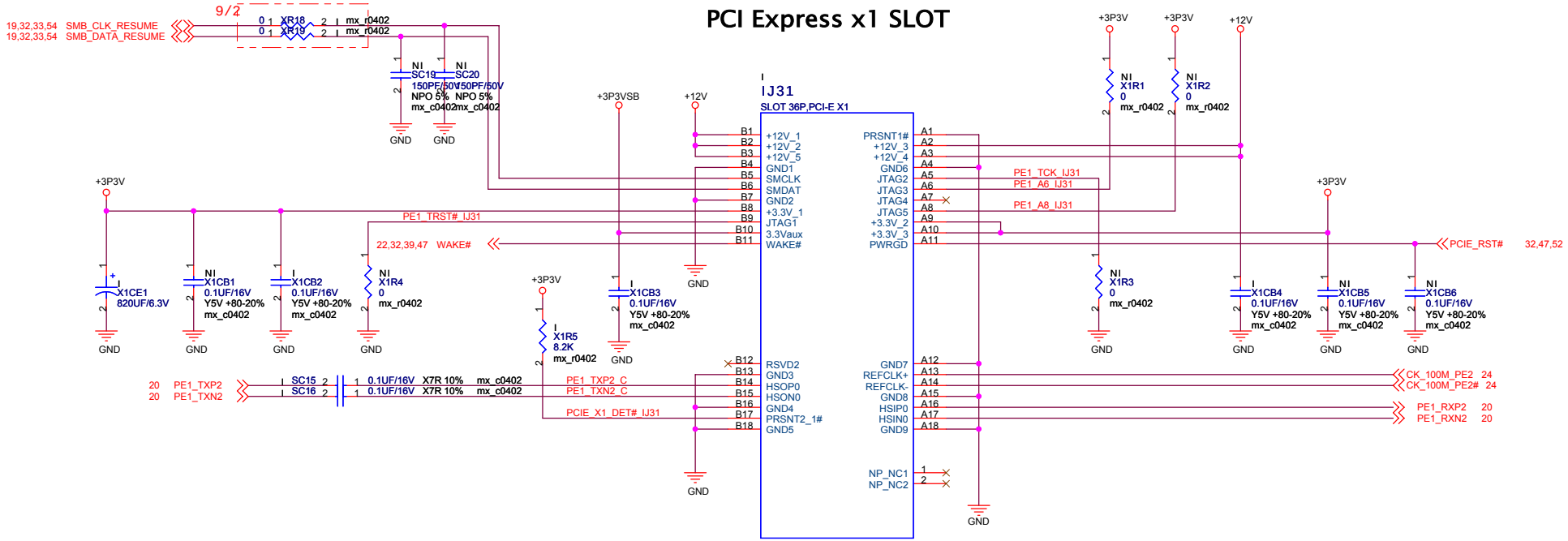


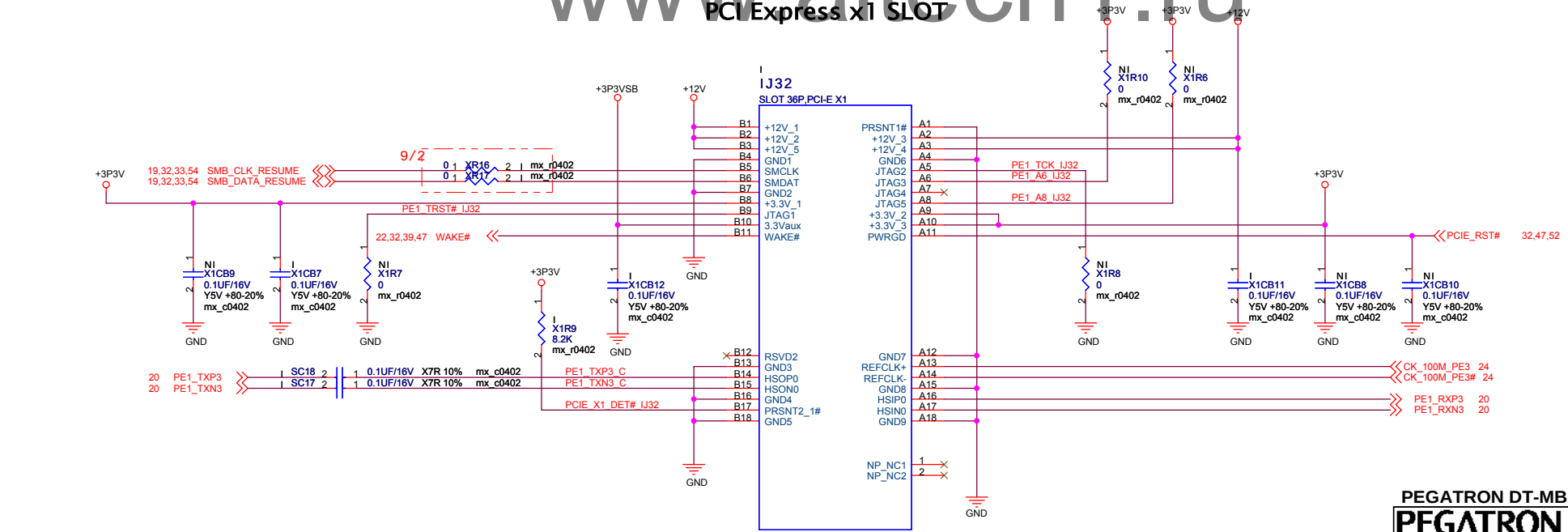
8/23：change P/N to 12X313164U0N

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : PCI EXPRESS X16 SLOT	
Pegatron Corp.	Engineer: Livy_Zhu	
Size: A3	Project Name: IPMSB-BE/CR	Rev: 1.00
Date: Friday, September 24, 2010	Sheet 32 of 83	







PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : PCI EXPRESS X1 SLOT

Pegatron Corp. Engineer: Livy_Zhu

Size	Project Name	Rev
A3	IPMSB-BE/CR	1.00

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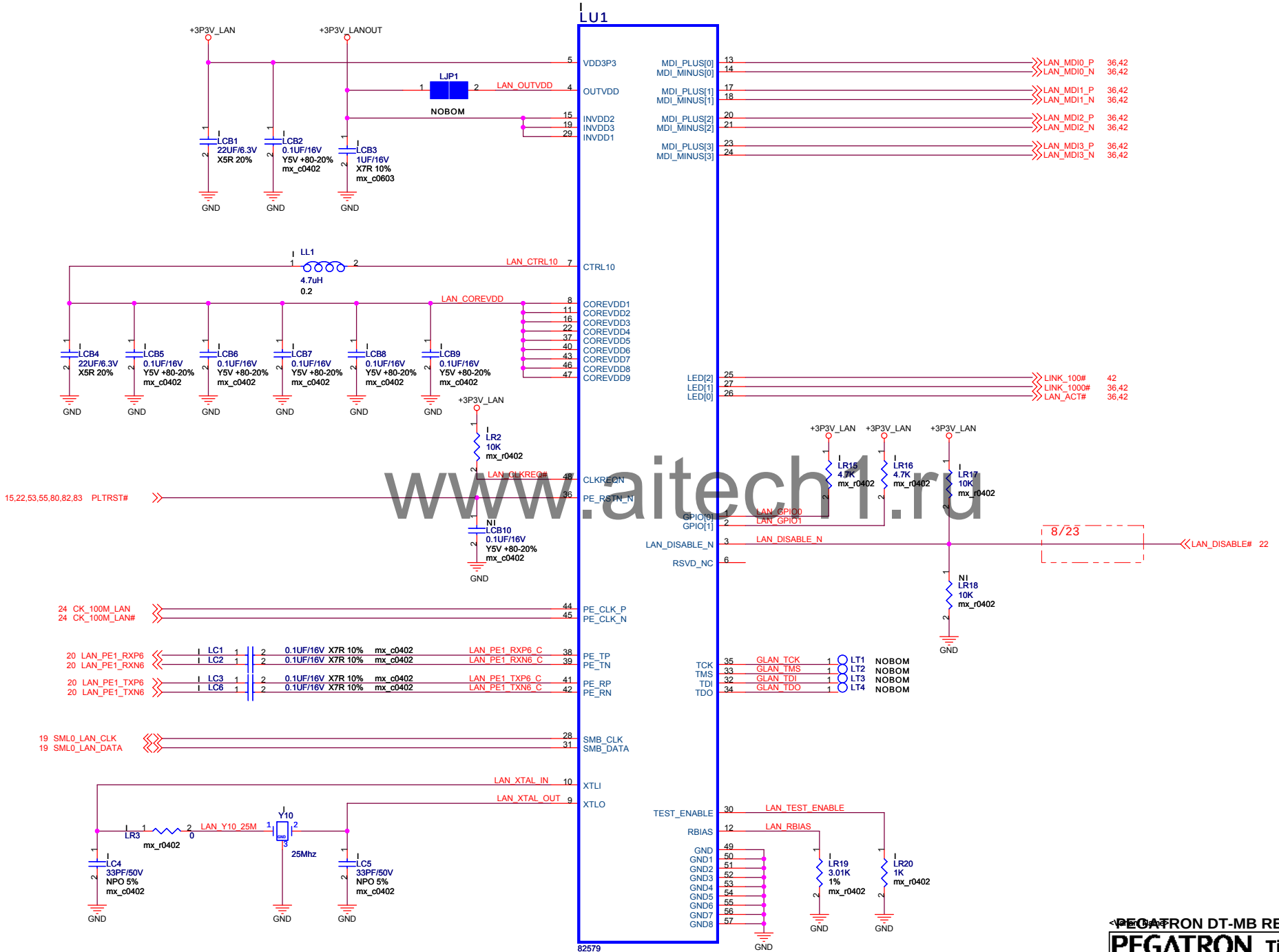

0901: Change PCH P/N directly to 0200-00J40IN
(ES2 C.S 908148 LEWISVILLE A-2 QMWM)

PEGATRON Title : LEWISVILLE 82579

Pegatron Corp. Engineer: Livy_Zhu

Size	Project Name	Rev
A3	IPMSB-BE/CR	1.00

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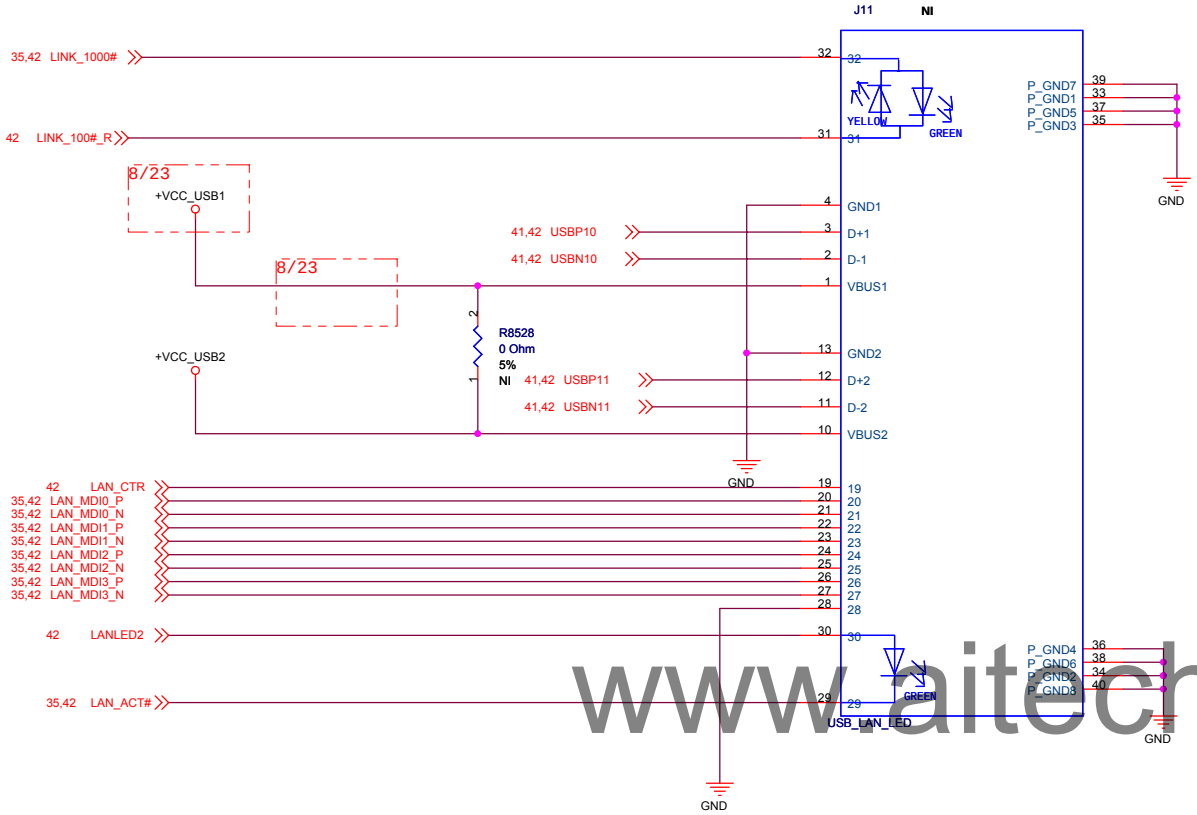

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : RJ45+USB2.0

PEGATRON CORP. Engineer: Livy_Zhu

Size	Project Name	Rev
A3	IPMSB-BE/CR	1.00

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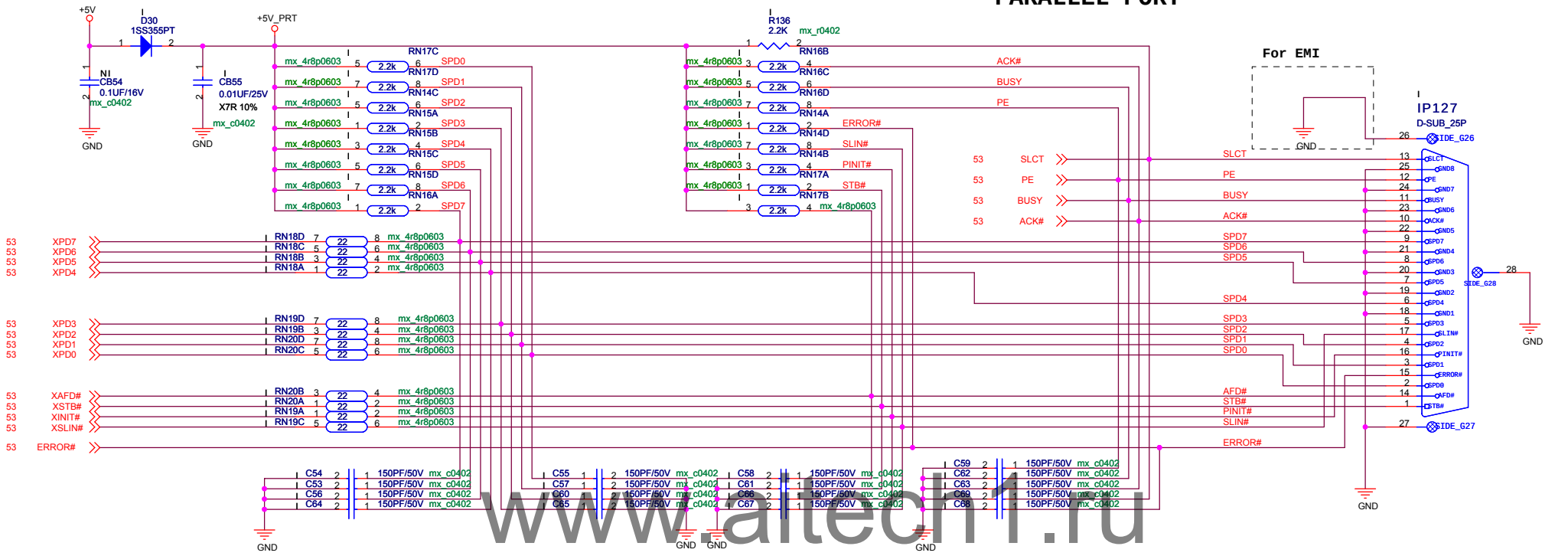
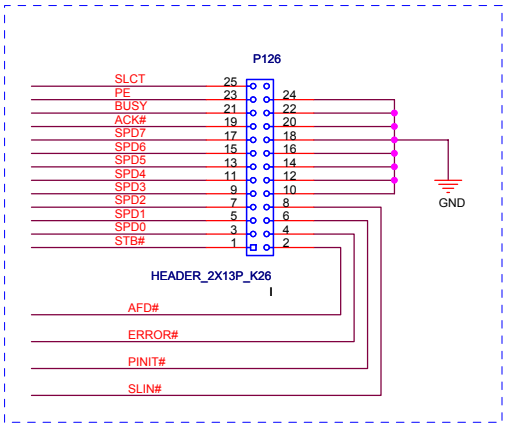
PARALLEL PORT



08/13: NI LPT header From Fab.B

8/18:
change LPT header from 12X60202DB10 to 12X60202DIW0

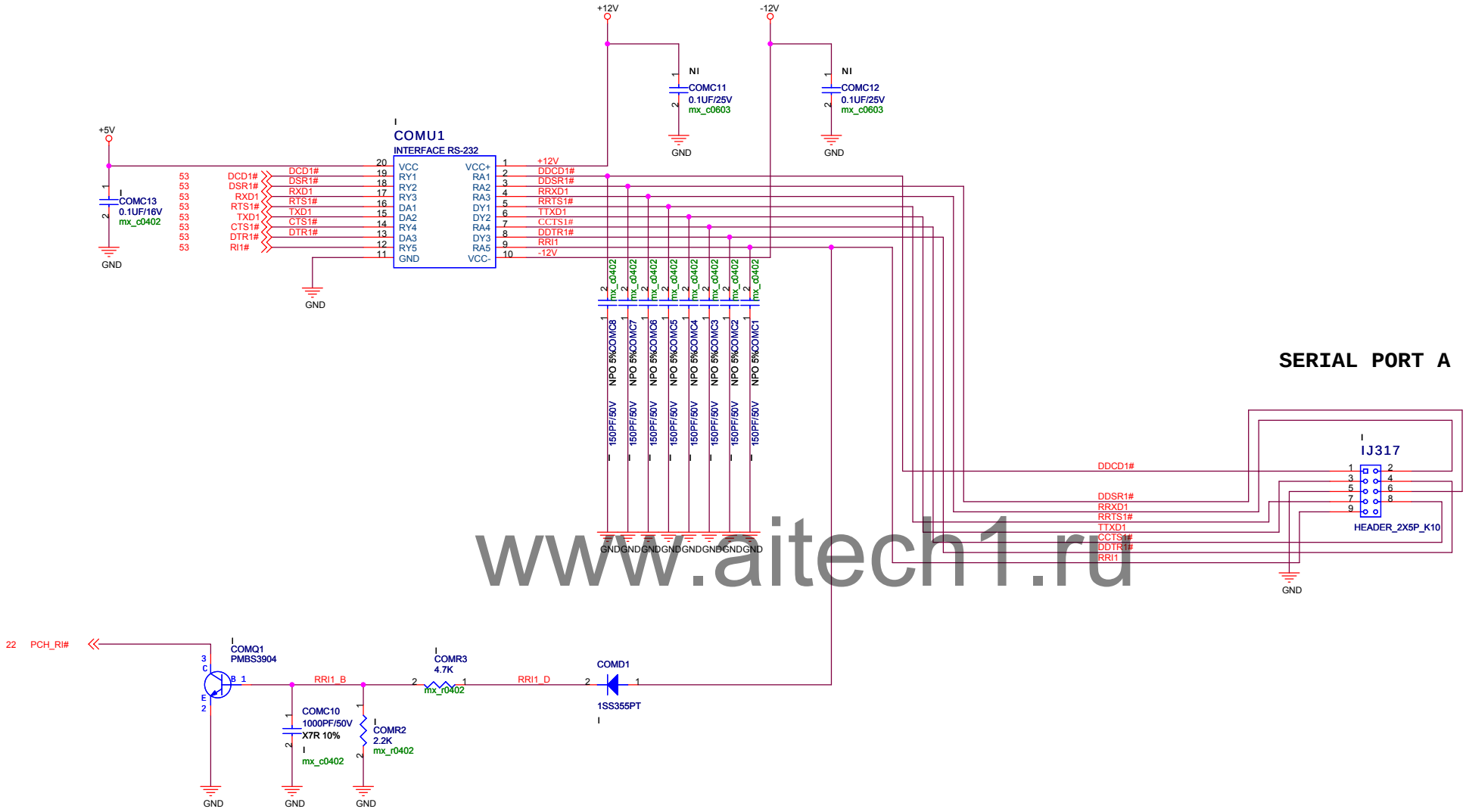


PEGATRON Title : PRINT PORT

Pegatron Corp. Engineer: Livy_Zhu

Size	Project Name	Rev
A3	IPMSB-BE/CR	1.00

Date: Friday, September 24, 2010 Sheet 37 of 83

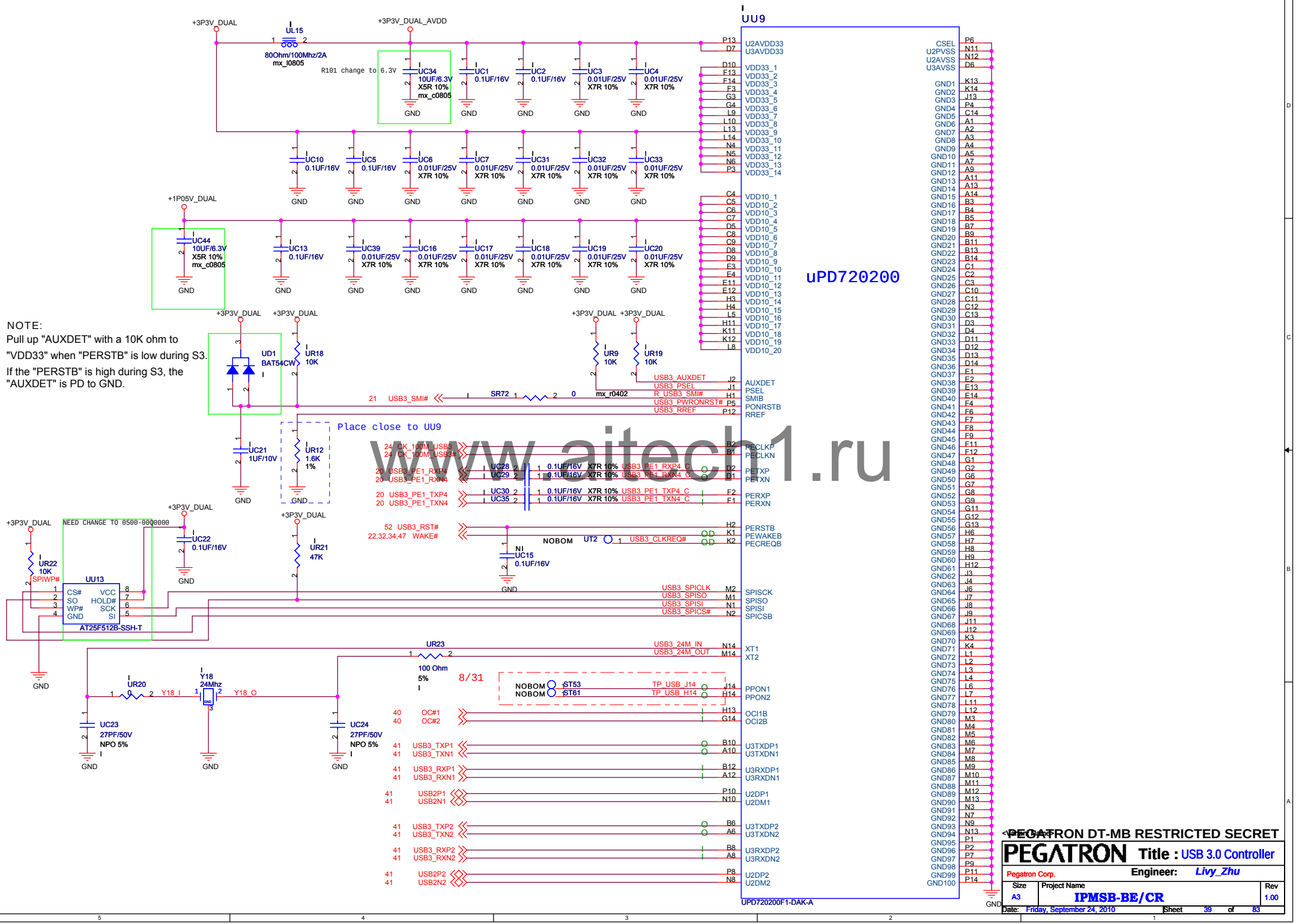


PEGATRON Title : SERIAL PORT

Pegatron Corp. Engineer: Livy_Zhu

Size	Project Name	Rev
A3	IPMSB-BE/CR	1.00

Date: Friday, September 24, 2010 Sheet 38 of 83



PEGATRON Title : USB 3.0 Controller

Pegatron Corp. Engineer: Livy_Zhu

Size	Project Name	Rev
A3	IPMSB-BE/CR	1.00

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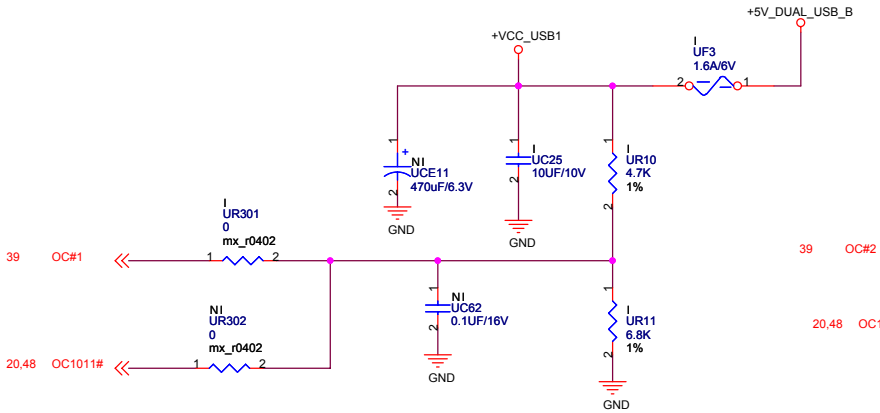
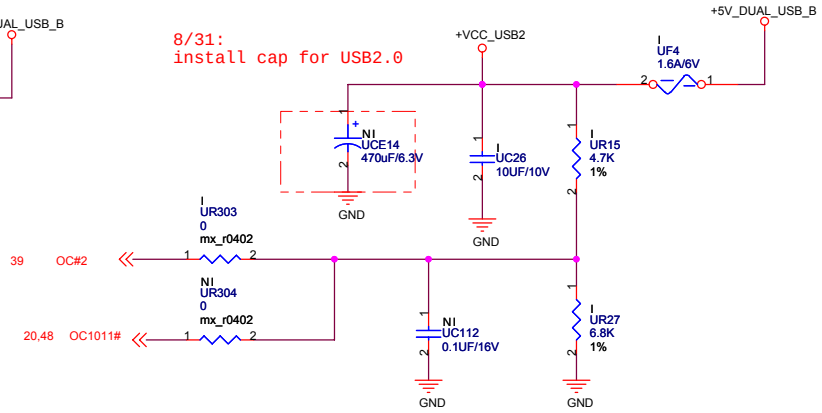
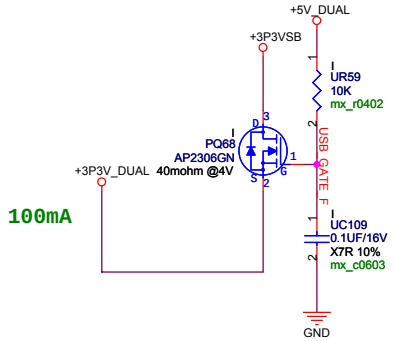






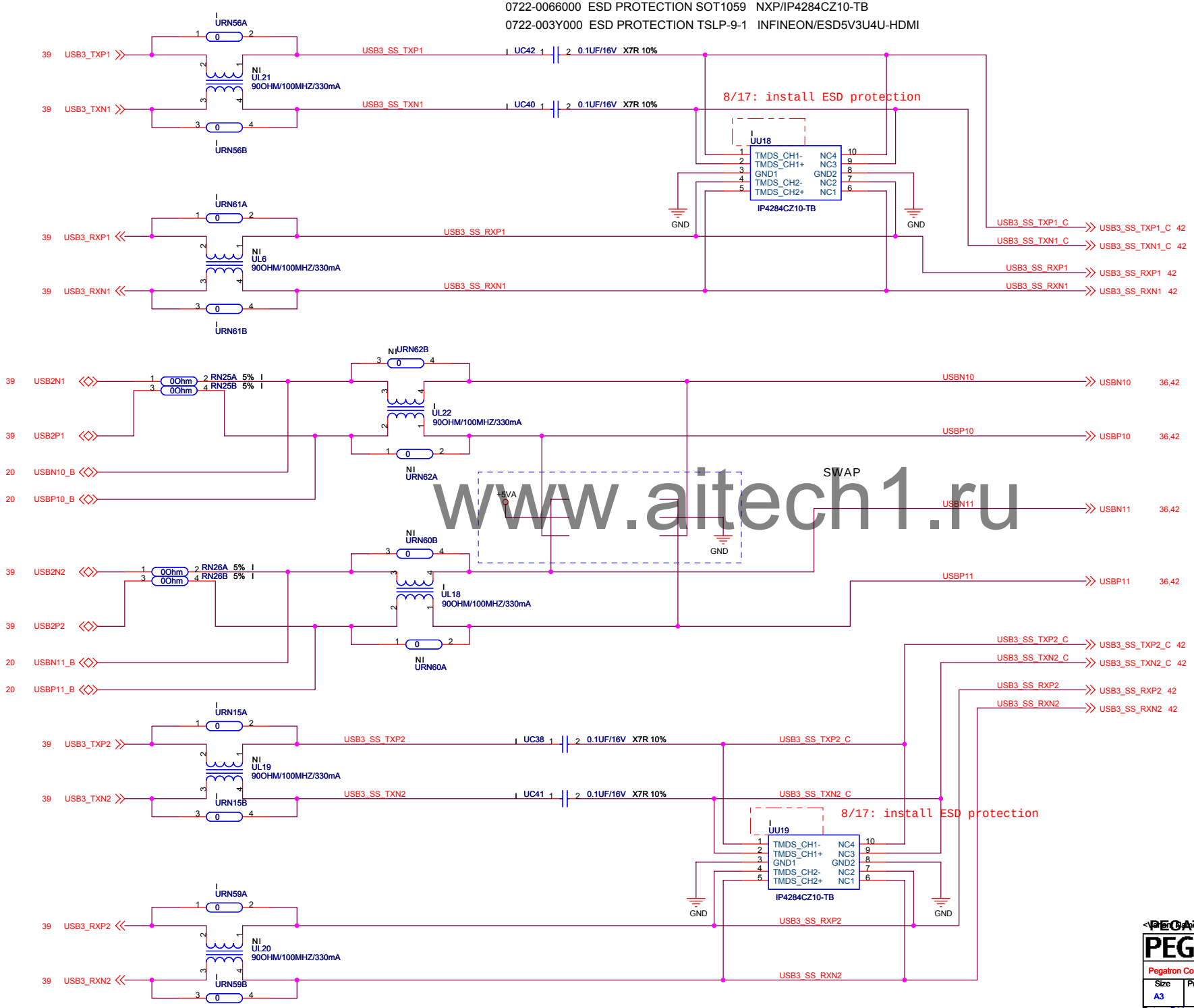
PEGATRON Title : USB 3.0 power

Pegatron Corp. Engineer: Livy_Zhu

Size	Project Name	Rev
A3	IPMSB-BE/CR	1.00

Date: Friday, September 24, 2010 Sheet 40 of 83

NOTE:
0722-0066000 ESD PROTECTION SOT1059 NXP/IP4284CZ10-TB
0722-003Y000 ESD PROTECTION TSLP-9-1 INFINEON/ESD5V3U4U-HDMI

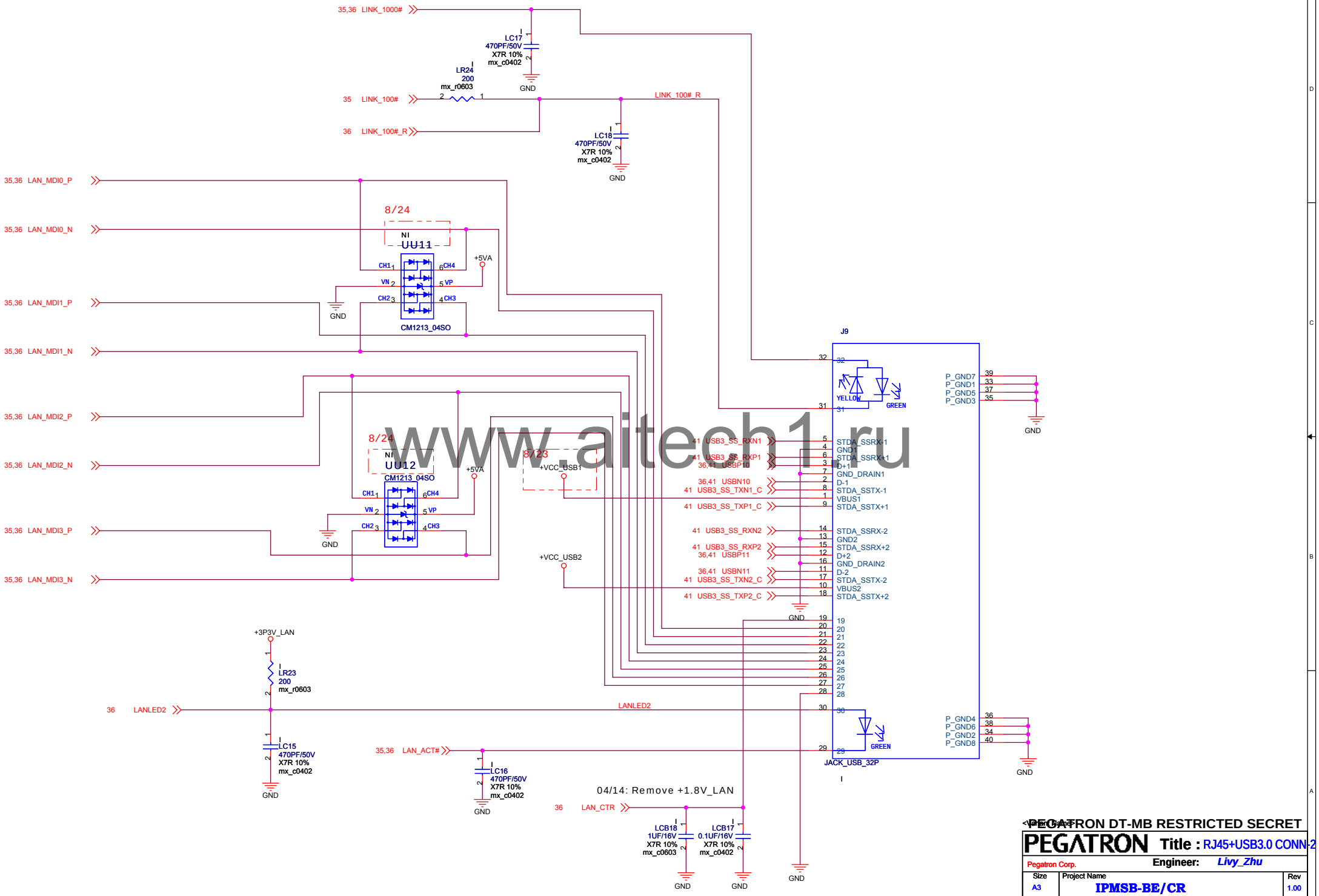


PEGATRON Title : RJ45+USB 3.0 CONN-1

Pegatron Corp. Engineer: Livy_Zhu

Size	Project Name	Rev
A3	IPMSB-BE/CR	1.00

Date: Friday, September 24, 2010 Sheet 41 of 83



PEGATRON Title : RJ45+USB3.0 CONN-2

Pegatron Corp. Engineer: Livy_Zhu

Size	Project Name	Rev
A3	IPMSB-BE/CR	1.00

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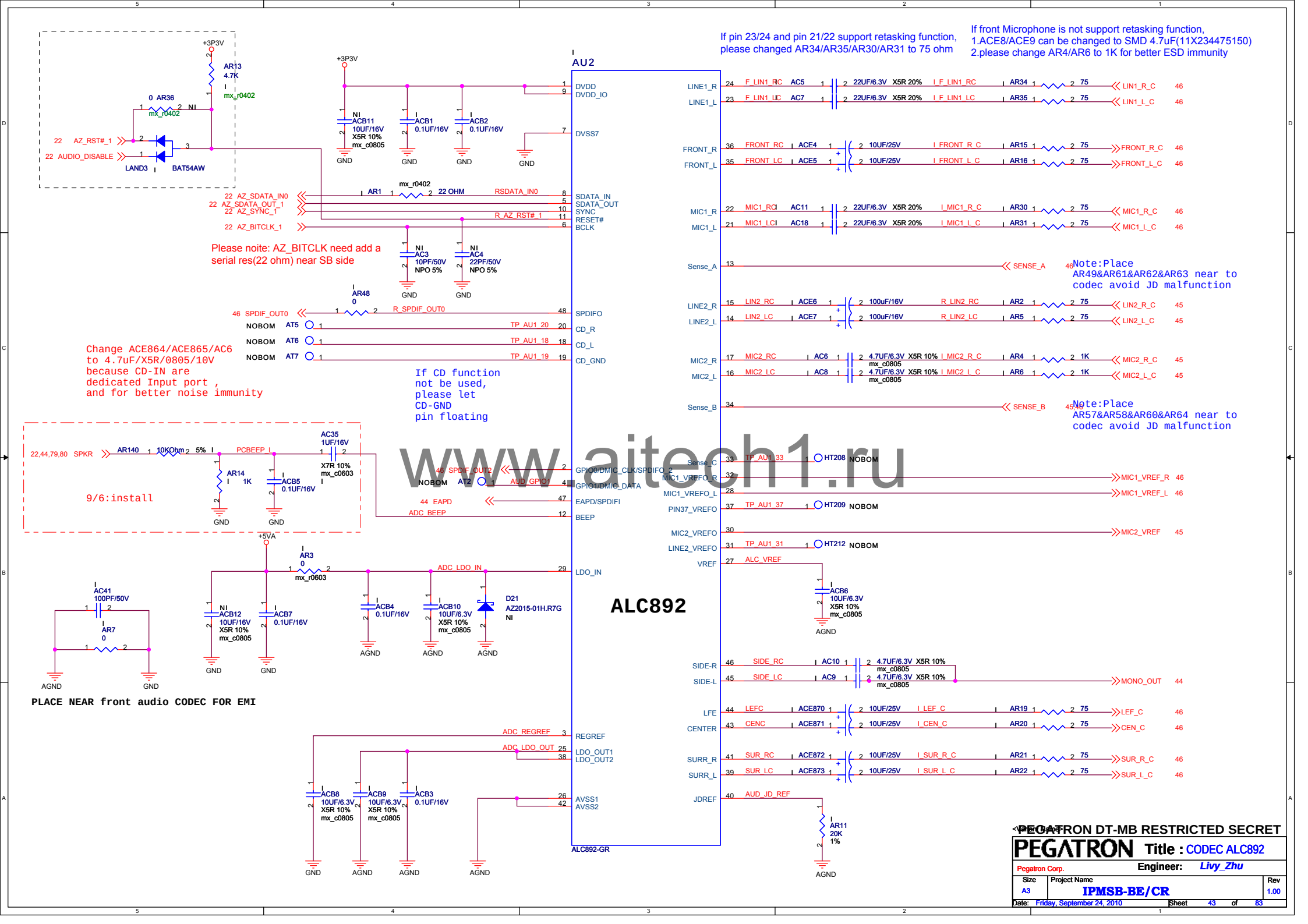
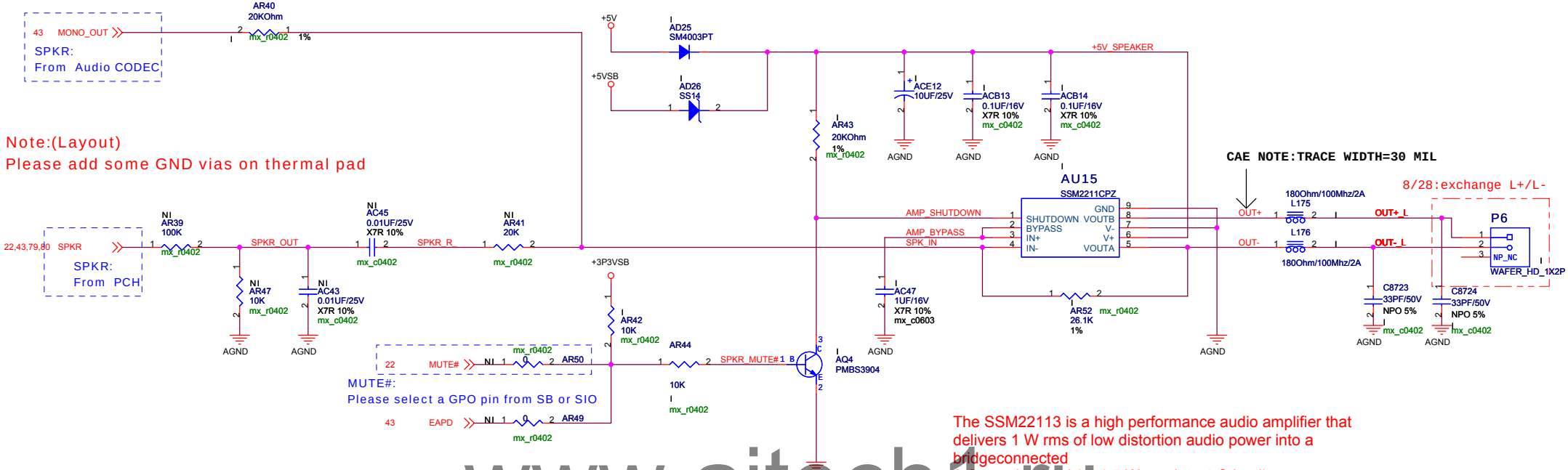

If pin 23/24 and pin 21/22 support retasking function, please changed AR34/AR35/AR30/AR31 to 75 ohm
If front Microphone is not support retasking function,
1.ACE8/ACE9 can be changed to SMD 4.7uF(11X234475150)
2.please change AR4/AR6 to 1K for better ESD immunity
AU2
ALC892
ALC892-GR
Please noite: AZ_BITCLK need add a serial res(22 ohm) near SB side
Change ACE864/ACE865/AC6 to 4.7uF/X5R/0805/10V because CD-IN are dedicated Input port , and for better noise immunity
If CD function not be used, please let CD-GND pin floating
Note:Place AR49&AR61&AR62&AR63 near to codec avoid JD malfunction
Note:Place AR57&AR58&AR60&AR64 near to codec avoid JD malfunction
9/6:install
PLACE NEAR front audio CODEC FOR EMI
www.aitech1.ru
PEGATRON DT-MB RESTRICTED SECRET
PEGATRON
Title : CODEC ALC892
Pegatron Corp.
Engineer: Livy_Zhu
Size A3
Project Name IPMSB-BE/CR
Rev 1.00
Date: Friday, September 24, 2010
Sheet 43 of 83

INTERNAL SPEAKER HEADER



The SSM22113 is a high performance audio amplifier that delivers 1 W rms of low distortion audio power into a bridgeconnected
8 Ω speaker load (or 1.5 W rms into 4 Ω load).

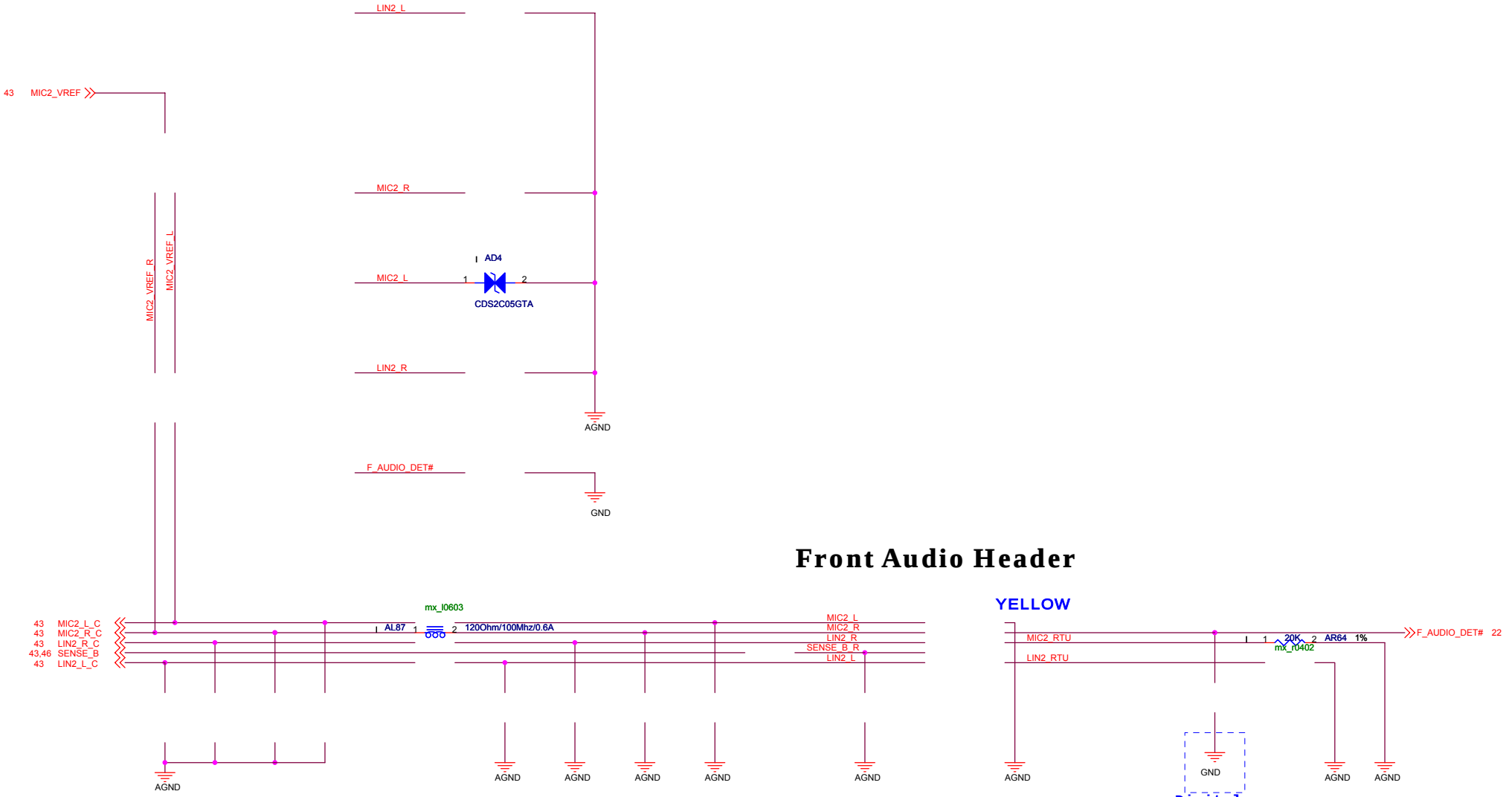
Net \ Level	H Level	L Level
Mute# Default	Non-Mute	Mute
AZ_GPIO0#	Non-Mute	Mute

PEGATRON Title : INTERNAL SPEAKER

Pegatron Corp. Engineer: Livy_Zhu

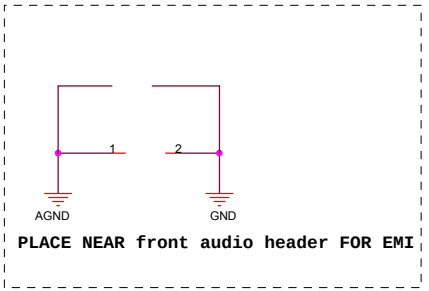
Size	Project Name	Rev
A3	IPMSB-BE/CR	1.00

Date: Friday, September 24, 2010 Sheet 44 of 83



Front Audio Header

If front HP-OUT is not support retasking,
these Vreference circuit can be removed.



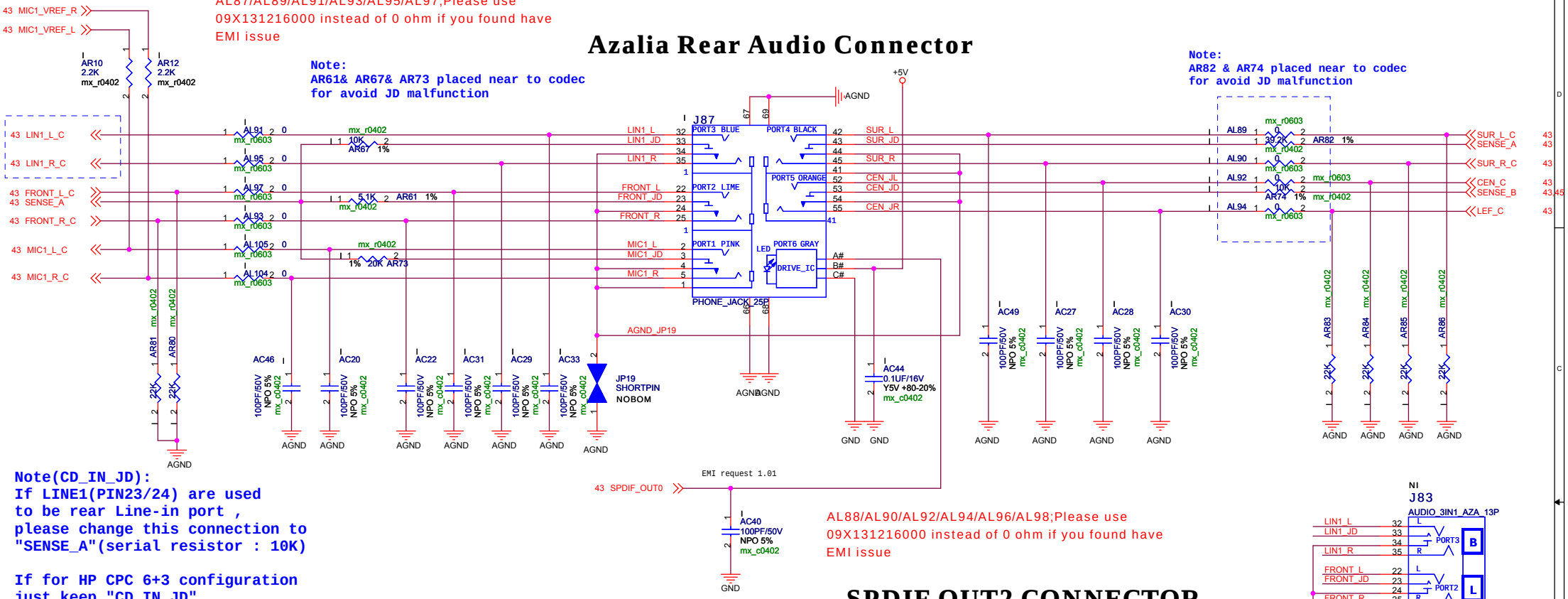
PEGATRON	Title : FRONT AUDIO HEADER	
Pegatron Corp.	Engineer: Livy_Zhu	
Size: A3	Project Name: IPMSB-BE/CR	Rev: 1.00
Date: Friday, September 24, 2010	Sheet 45 of 83	

Azalia Rear Audio Connector

AL87/AL89/AL91/AL93/AL95/AL97;Please use 09X131216000 instead of 0 ohm if you found have EMI issue

Note:
AR61& AR67& AR73 placed near to codec for avoid JD malfunction

Note:
AR82 & AR74 placed near to codec for avoid JD malfunction

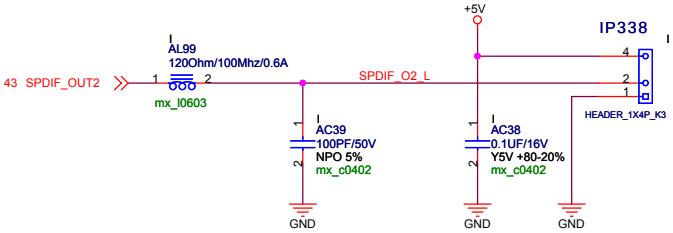


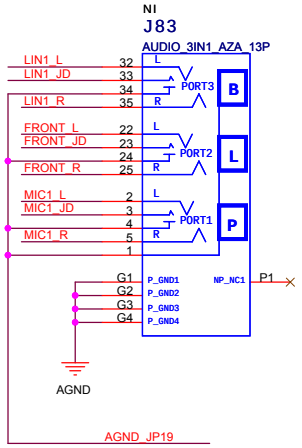
Note(CD_IN_JD):
If LINE1(PIN23/24) are used to be rear Line-in port , please change this connection to "SENSE_A"(serial resistor : 10K)

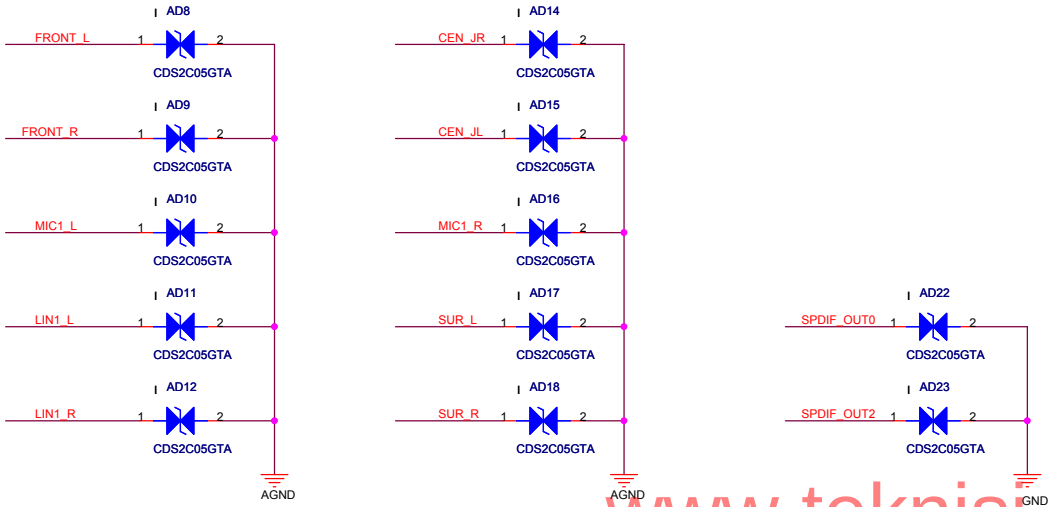
If for HP CPC 6+3 configuration just keep "CD_IN_JD"

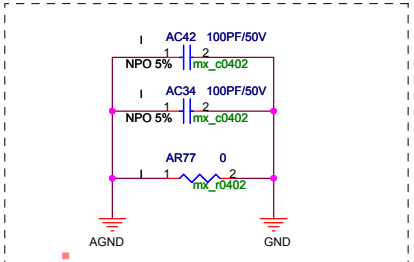
AL88/AL90/AL92/AL94/AL96/AL98;Please use 09X131216000 instead of 0 ohm if you found have EMI issue

SPDIF OUT2 CONNECTOR

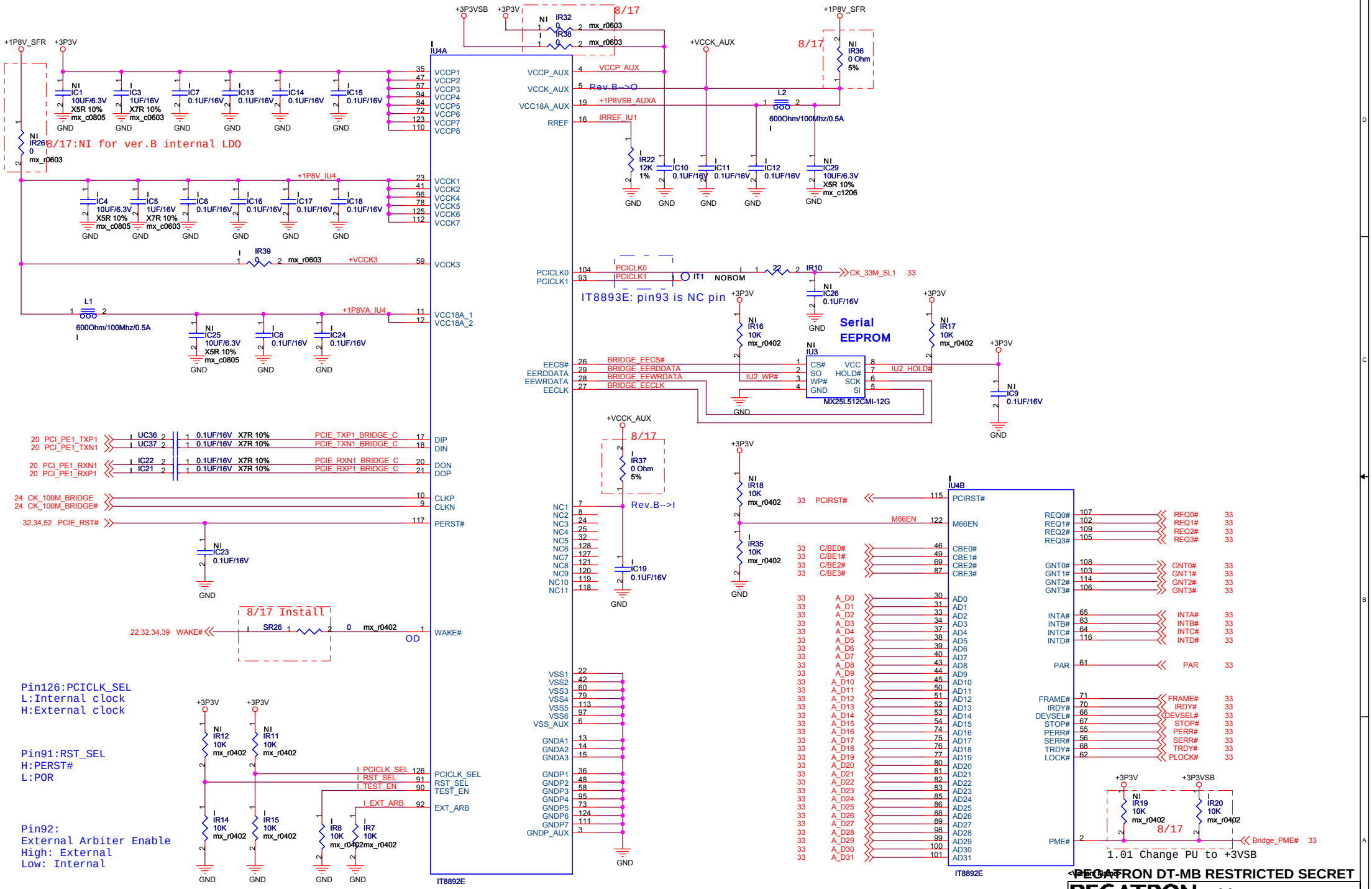




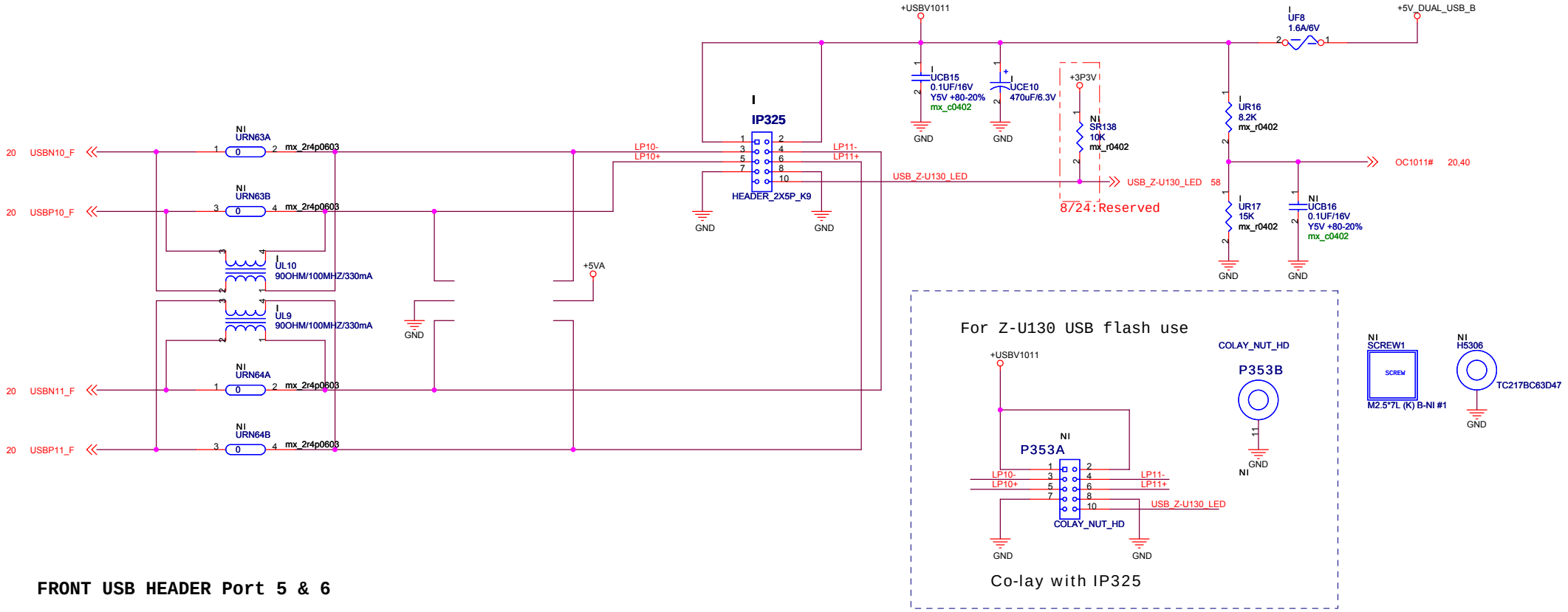




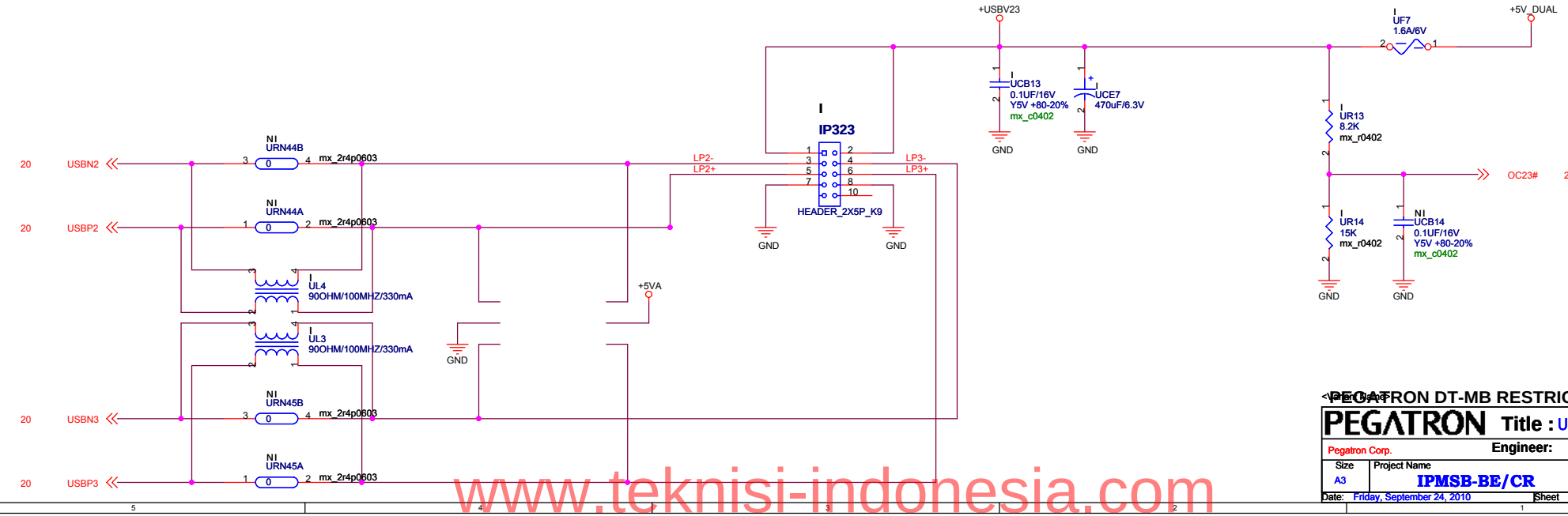
PEGATRON	Title : REAL AUDIO CONN	
Pegatron Corp.	Engineer: Livy_Zhu	
Size: A3	Project Name: IPMSB-BE/CR	Rev: 1.00
Date: Friday, September 24, 2010	Sheet 46 of 83	



FRONT USB HEADER Port 7 & 8



FRONT USB HEADER Port 5 & 6



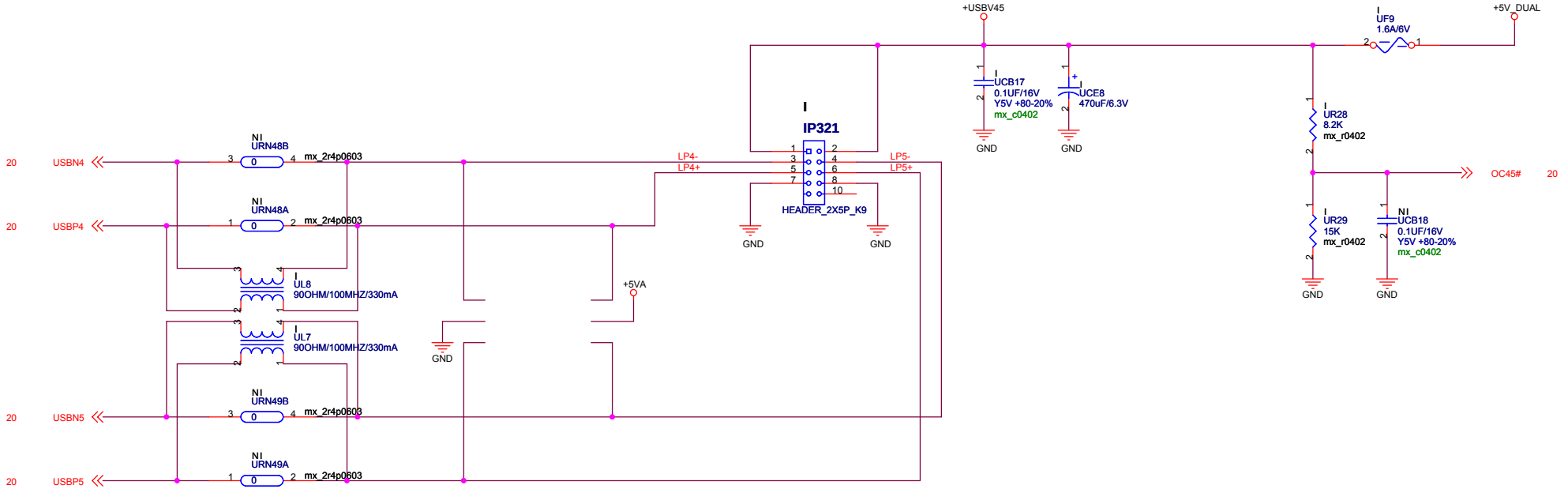
PEGATRON Title : USB HEADER-1

Pegatron Corp. Engineer: Livy_Zhu

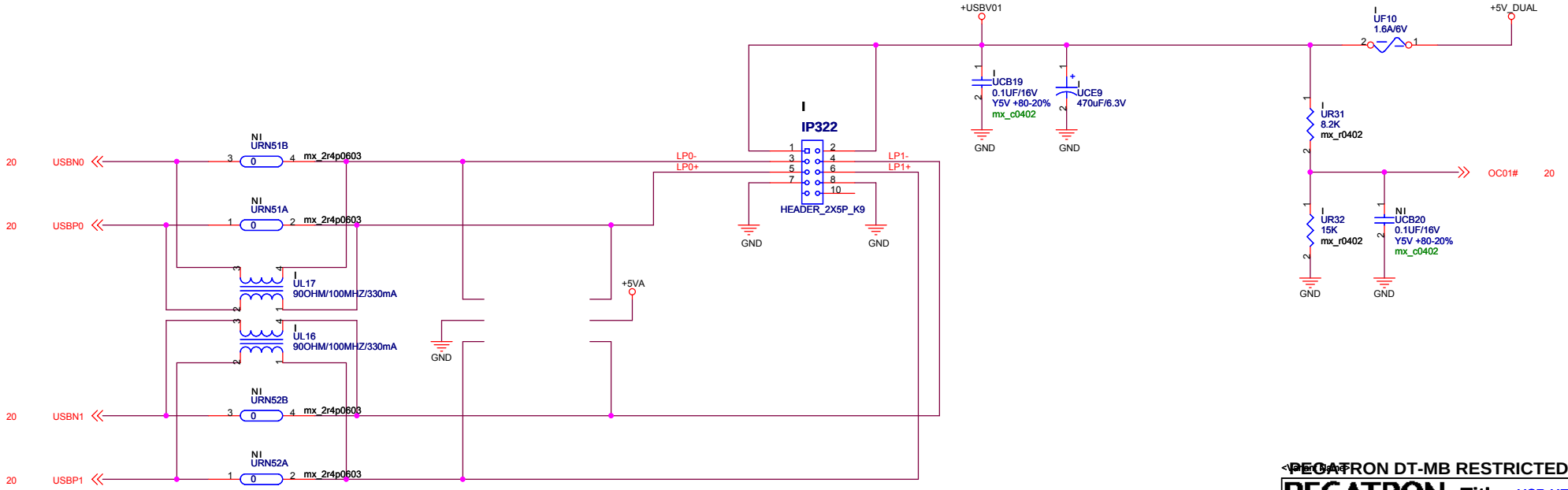
Size	Project Name	Rev
A3	IPMSB-BE/CR	1.00

Date: Friday, September 24, 2010 Sheet 48 of 83

FRONT USB HEADER Port 1 & 2



FRONT USB HEADER Port 3 & 4

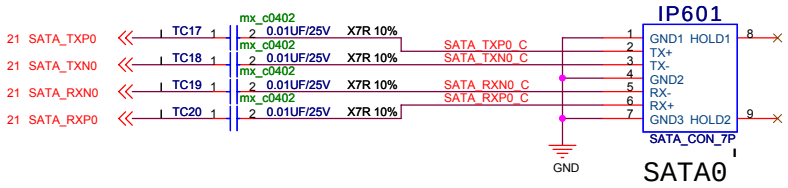


PEGATRON Title : USB HEADER-2

Pegatron Corp. Engineer: Livy_Zhu

Size	Project Name	Rev
A3	IPMSB-BE/CR	1.00

Date: Friday, September 24, 2010 Sheet 49 of 83



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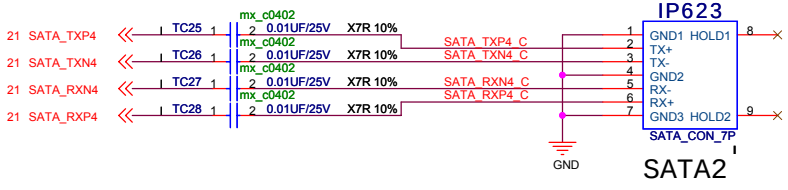

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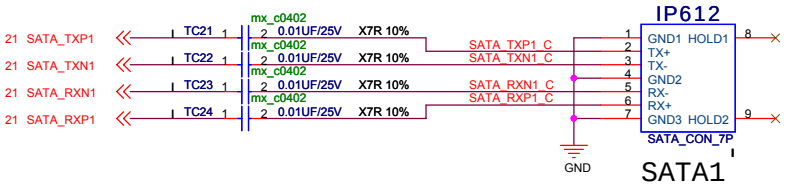

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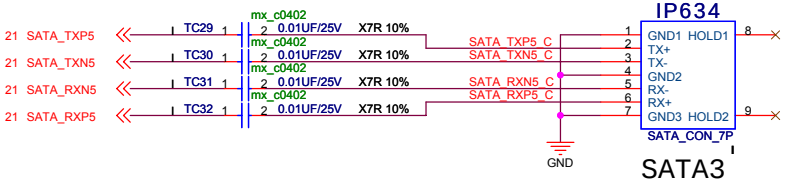


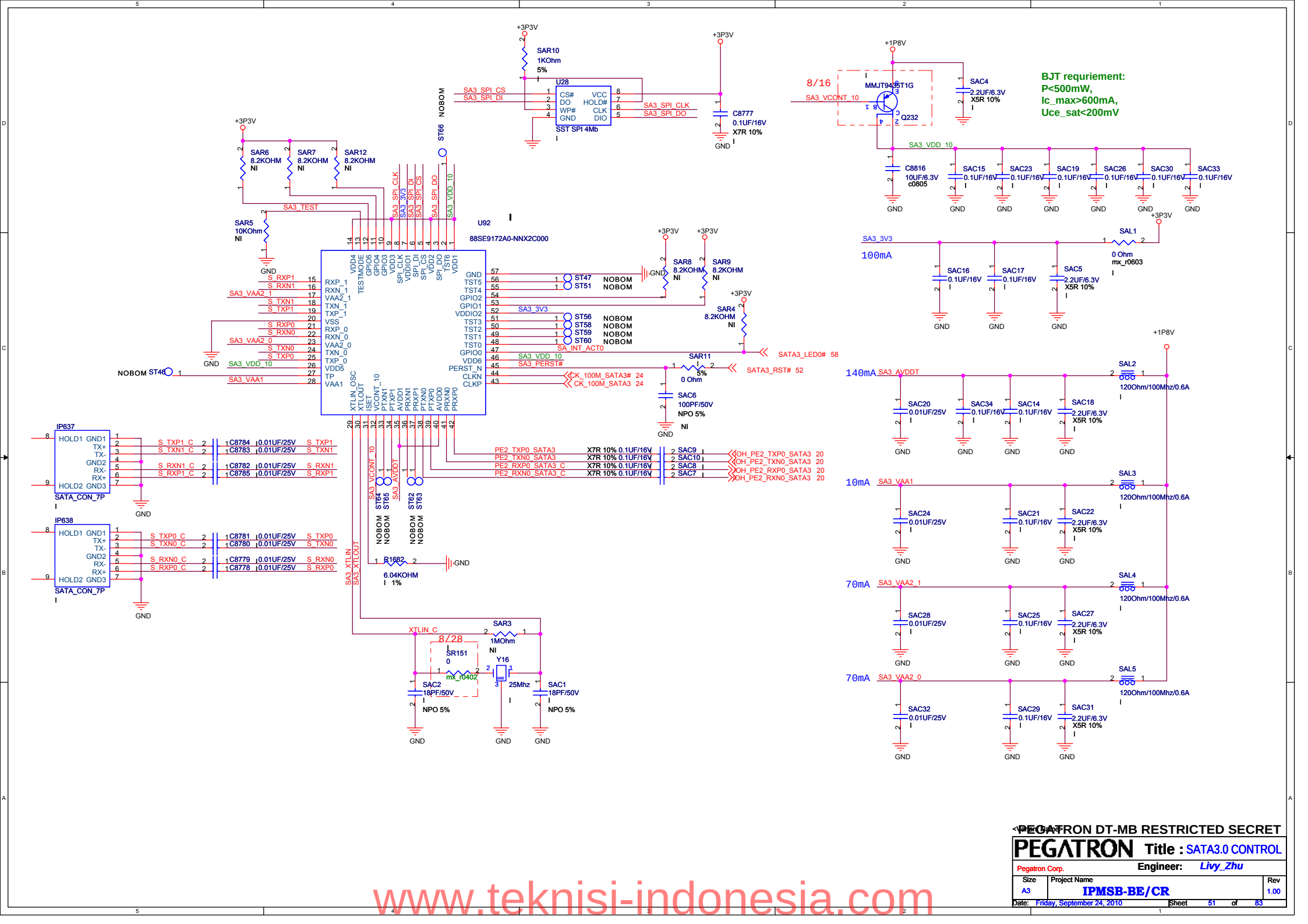
COLOR = BLACK

PEGATRON Title : SATA CONN

Pegatron Corp. Engineer: Livy_Zhu

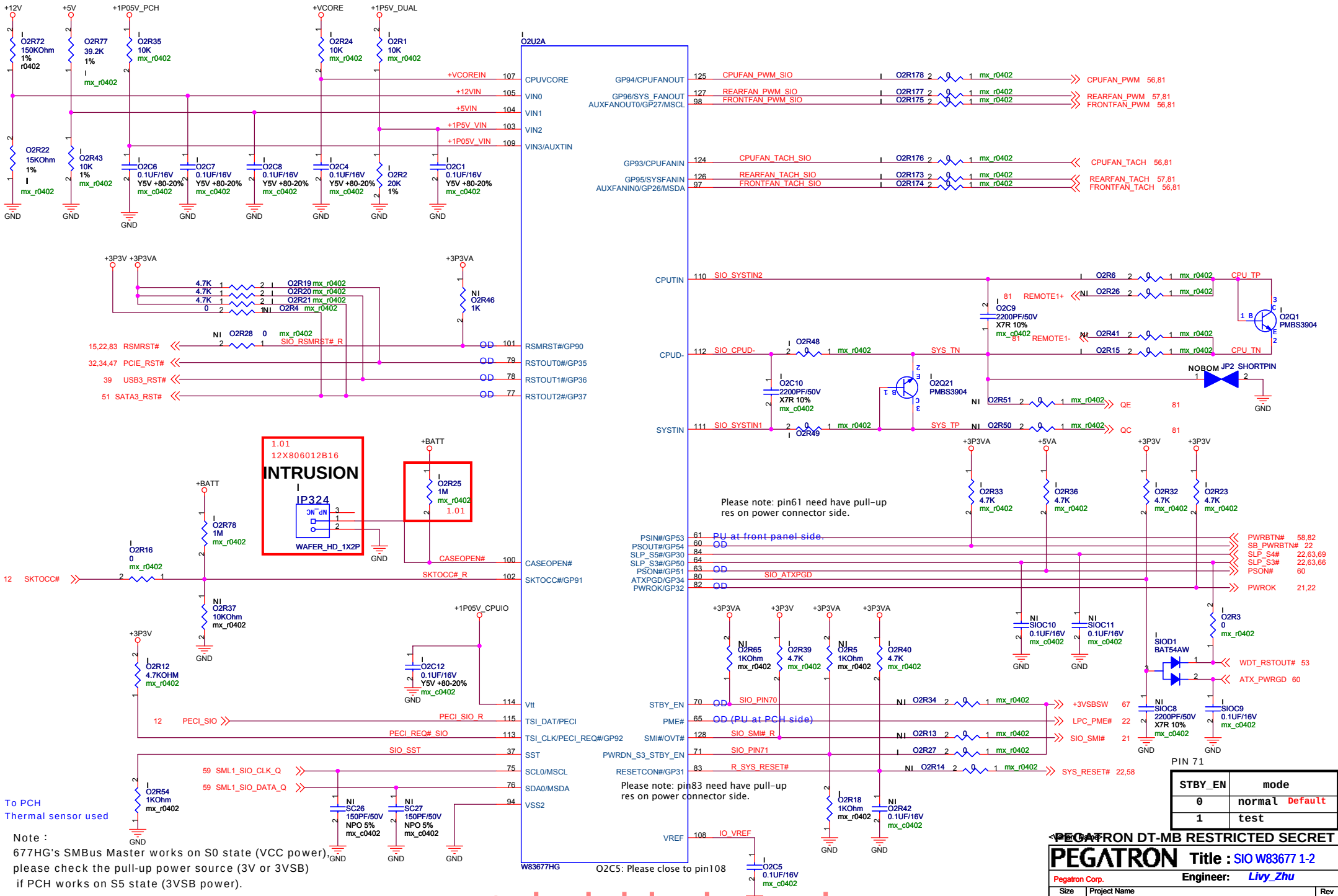
Size	Project Name	Rev
A3	IPMSB-BE/CR	1.00

Date: Friday, September 24, 2010 Sheet 50 of 83



Voltage avoid over 2.048V or less than 0V
Please add those divider res if you need to monitor the voltage with +5V or +12V

Please do not leave pin 103 VCORE_REFIN floating.
Otherwise, pin 63 PSON# will be affected and the system cannot be booted.



PEGATRON Title : SIO W83677 1-2
Pegatron Corp. Engineer: Livy_Zhu
Size A3 | Project Name IPMSB-BE/CR | Rev 1.00
Date: Friday, September 24, 2010 | Sheet 52 of 83

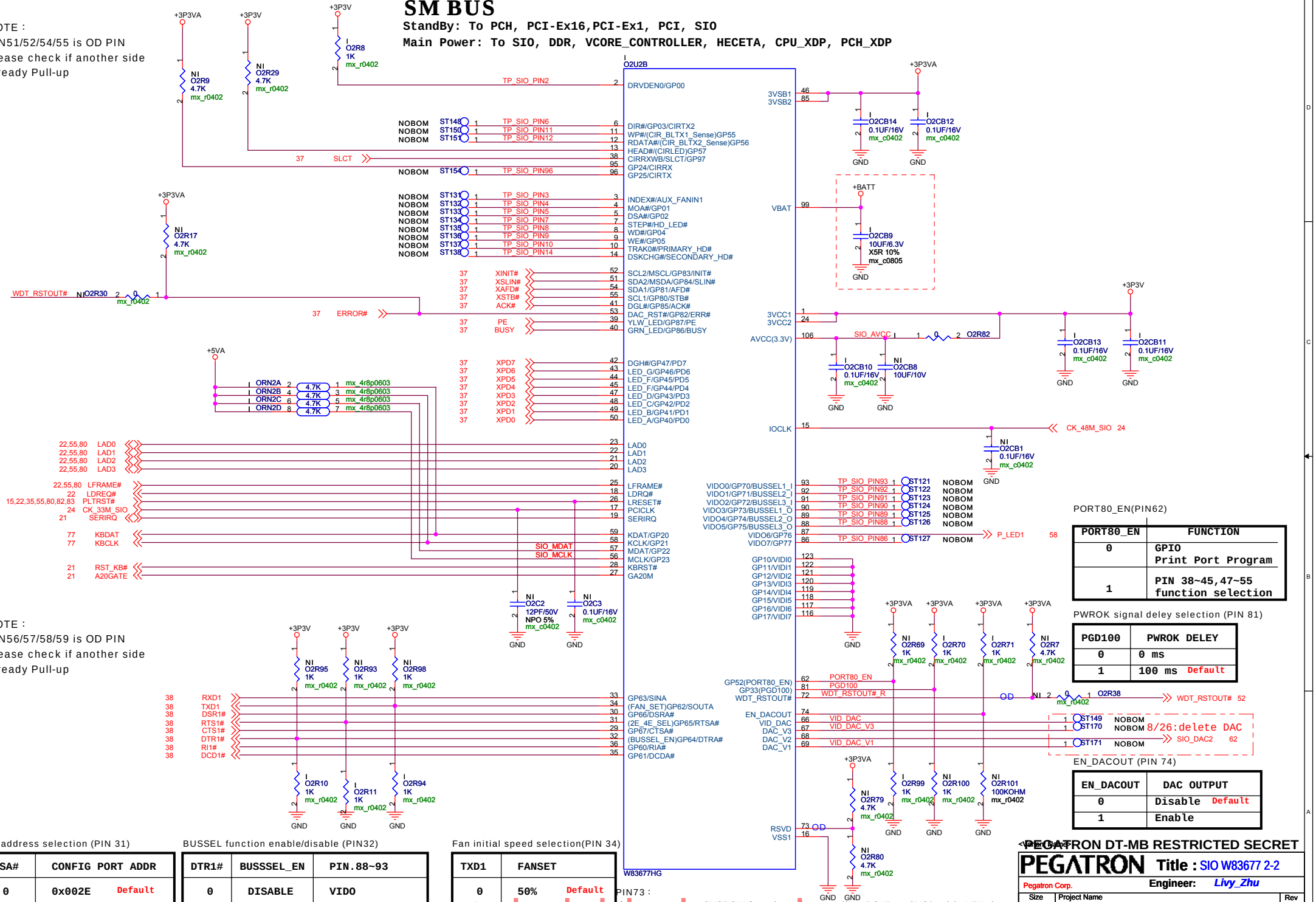
SM BUS

StandBy: To PCH, PCI-Ex16,PCI-Ex1, PCI, SIO

Main Power: To SIO, DDR, VCORE_CONTROLLER, HECETA, CPU_XDP, PCH_XDP

NOTE :
PIN51/52/54/55 is OD PIN
Please check if another side already Pull-up

NOTE :
PIN56/57/58/59 is OD PIN
Please check if another side already Pull-up



PORT80_EN(PIN62)

PORT80_EN	FUNCTION
0	GPIO Print Port Program
1	PIN 38~45,47~55 function selection

PWROK signal deley selection (PIN 81)

PGD100	PWROK DELEY
0	0 ms
1	100 ms Default

EN_DACOUT (PIN 74)

EN_DACOUT	DAC OUTPUT
0	Disable Default
1	Enable

LPC address selection (PIN 31)

RTSA#	CONFIG PORT ADDR
0	0x002E Default
1	0x004E

BUSSEL function enable/disable (PIN32)

DTR1#	BUSSSEL_EN	PIN.88~93
0	DISABLE	VIDO
1	ENABLE	BUSSEL IN/OUT

Fan initial speed selection(PIN 34)

TXD1	FANSET
0	50% Default
1	100%

PIN73 :
If we want to use 3VSBSW function, please pull up RSVD to 3VSB with 4.7Kohm
Otherwise pull down RSVD with 4.7Kohm, then pin70 is STBY_EN function.

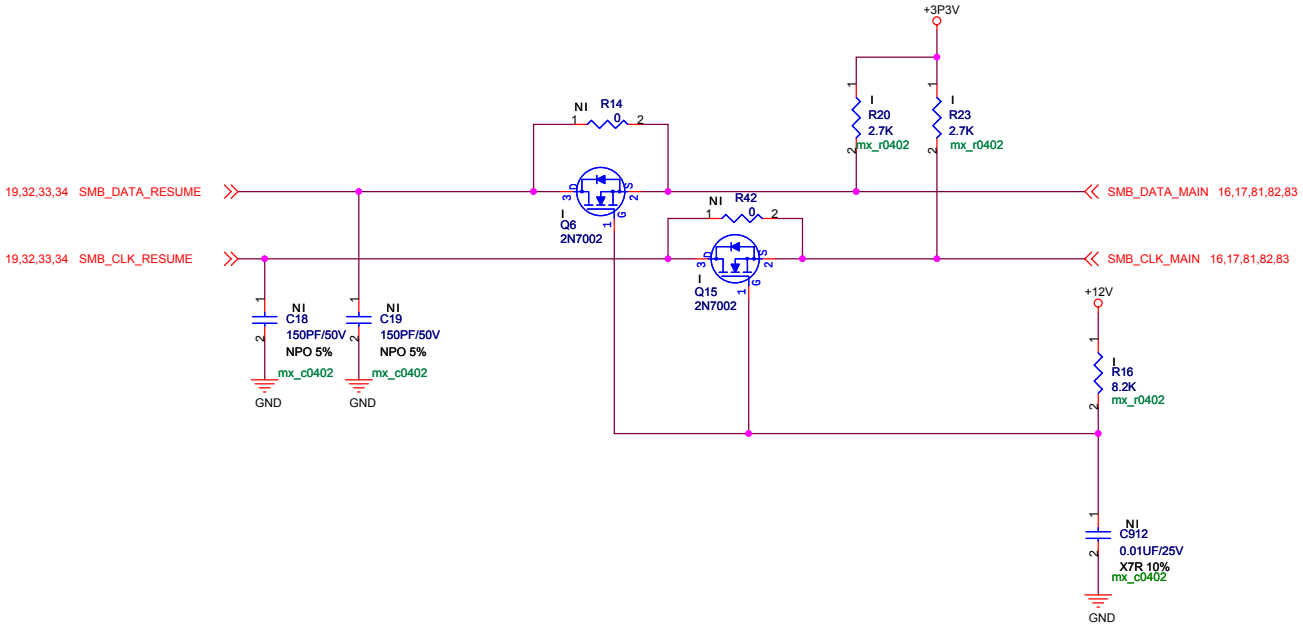
PEGATRON Title : SIO W83677 2-2

Pegatron Corp. Engineer: Livy_Zhu

Size	Project Name	Rev
A3	IPMSB-BE/CR	1.00

Date: Friday, September 24, 2010 Sheet 53 of 83

SM BUS Control



PEGATRON Title : SMBUS CONTROL

Pegatron Corp. Engineer: Livy_Zhu

Size	Project Name	Rev
A3	IPMSB-BE/CR	1.00

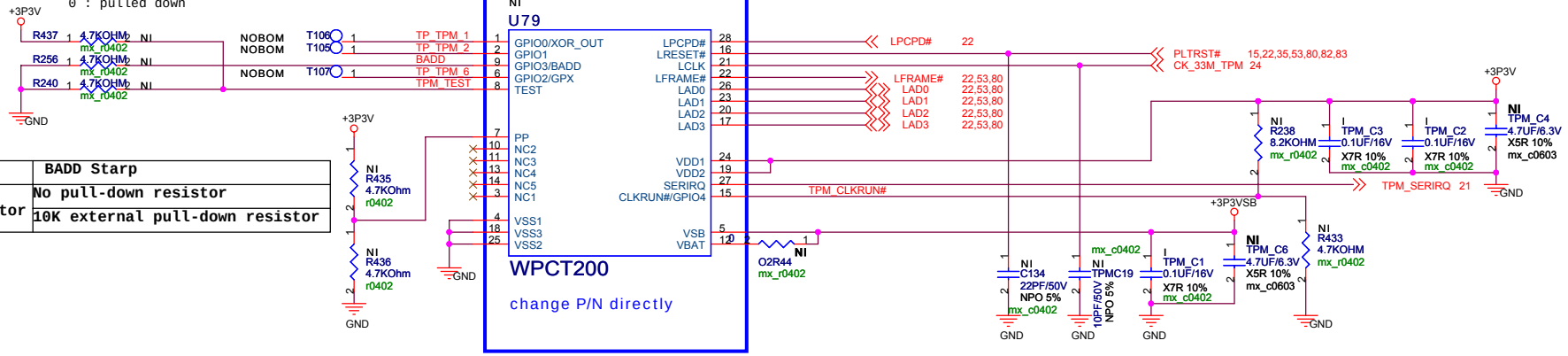
Date: Friday, September 24, 2010 Sheet 54 of 83

08/13: NI TPM From Fab.B

BADD	SELECTION
0	EEh-EFh
1	7Eh-7Fh

1 : left open
0 : pulled down

change to W210I
023E-000D000



Test Mode	Test Starp	BADD Starp
XOR tree	4.7K external pull-up resistor	No pull-down resistor
TRI-state		10K external pull-down resistor

PEGATRON Title : TPM

Pegatron Corp. Engineer: Livy_Zhu

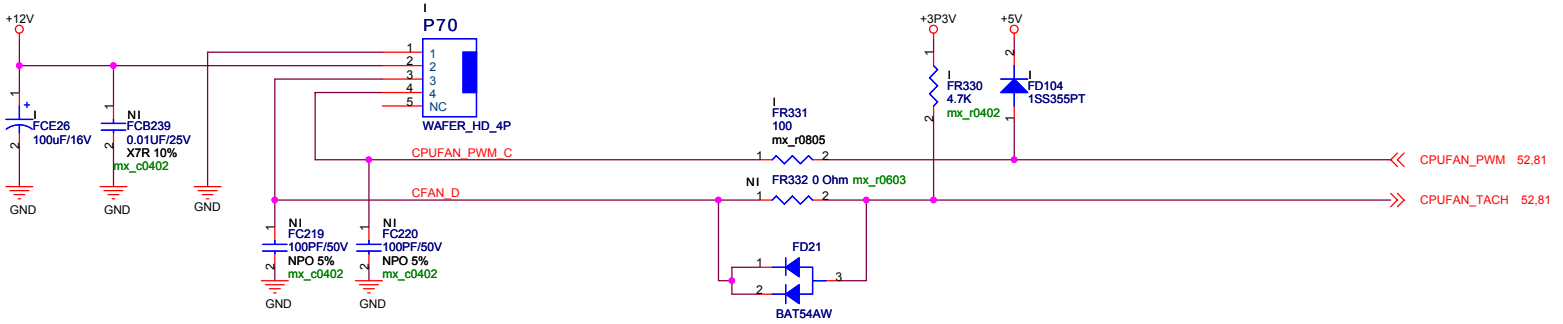
Size	Project Name	Rev
A3	IPMSB-BE/CR	1.00

Date: Friday, September 24, 2010 Sheet 55 of 83

CPU FAN

COLOR: WHITE

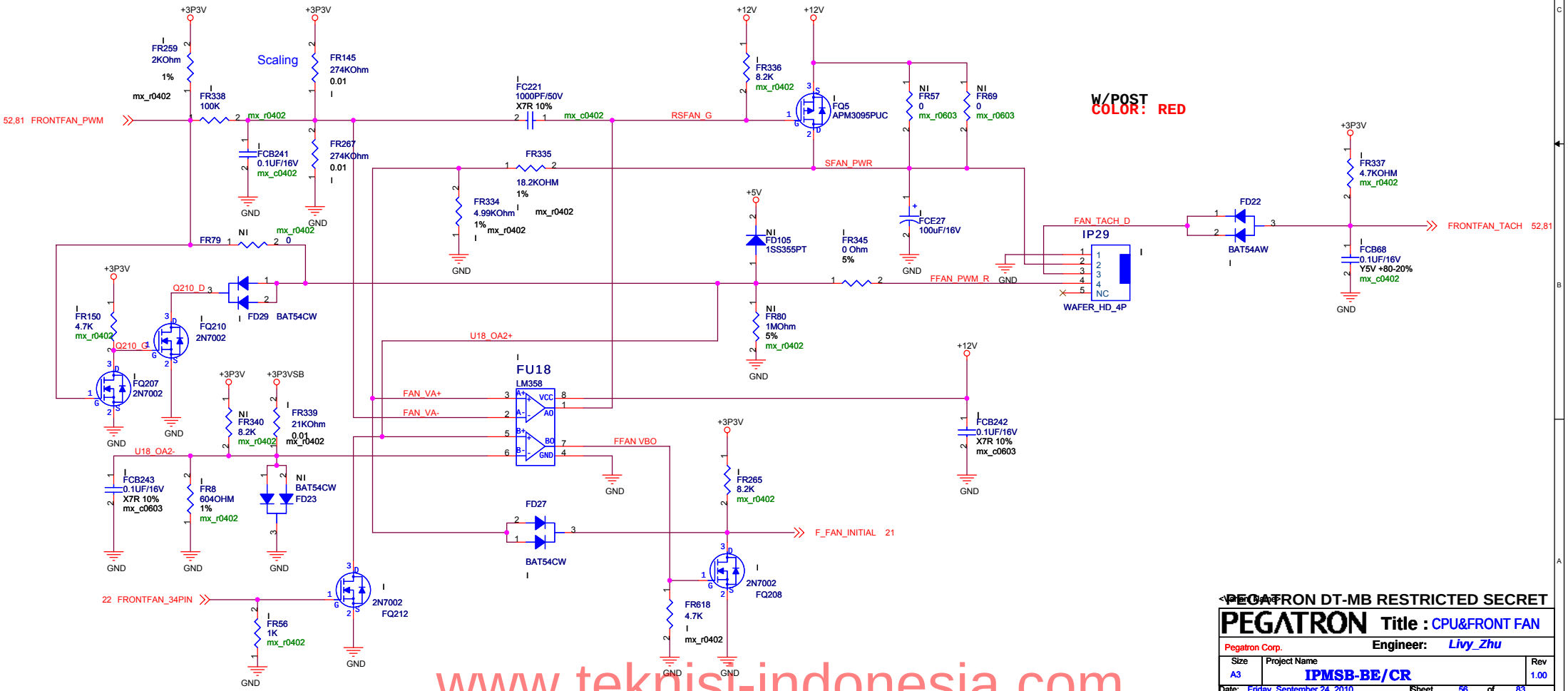
W/POST



FRONT FAN

W/POST

COLOR: RED



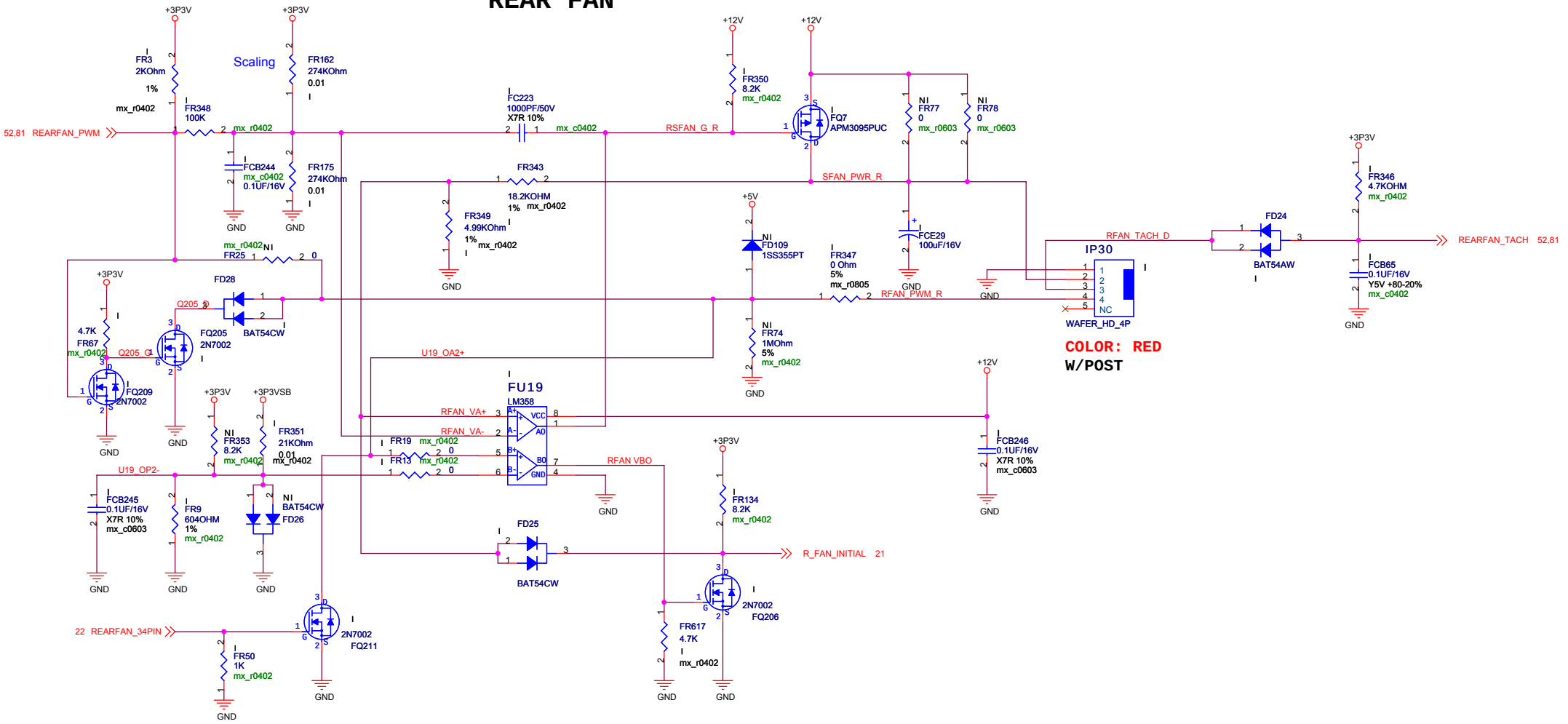
PEGATRON Title : CPU&FRONT FAN

Pegatron Corp. Engineer: Livy_Zhu

Size	Project Name	Rev
A3	IPMSB-BE/CR	1.00

Date: Friday, September 24, 2010 Sheet 56 of 83

REAR FAN



PEGATRON Title : REAR FAN CIRCUIT

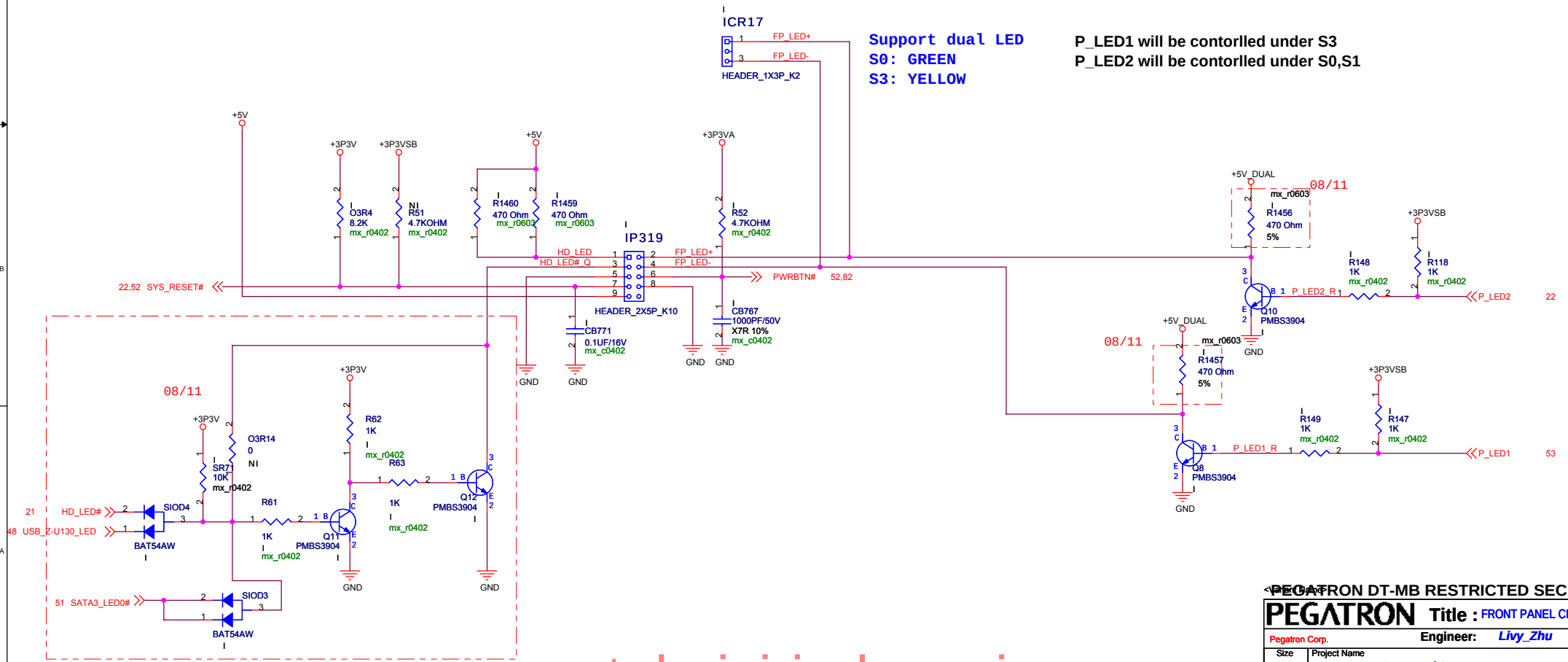
Pegatron Corp. Engineer: Livy_Zhu

Size	Project Name	Rev
A3	IPMSB-BE/CR	1.00

Date: Friday, September 24, 2010 Sheet 57 of 83

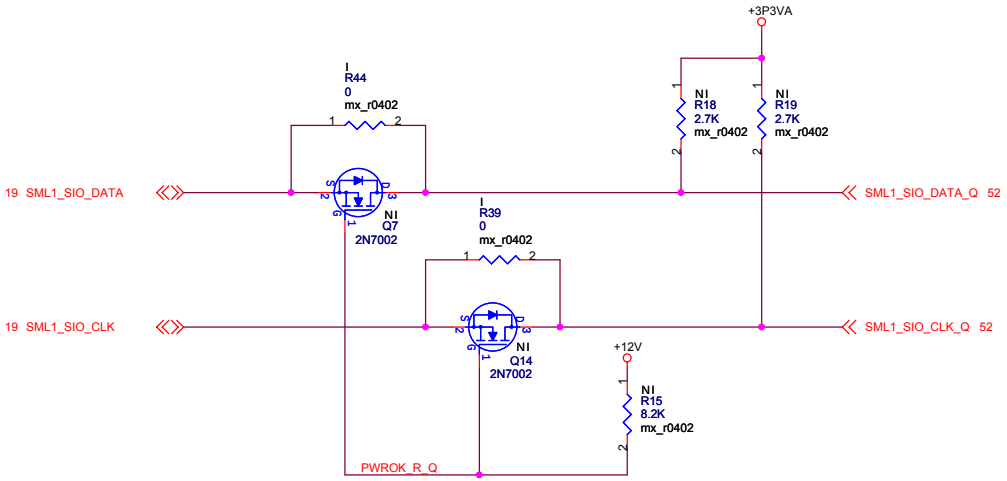
FRONT PANEL / LED CIRCUITRY

NOTE:
PWRBTN# of PCH is internally pulled-up in PCH to 3.3 V standby through a weak pull-up 24Kohm.

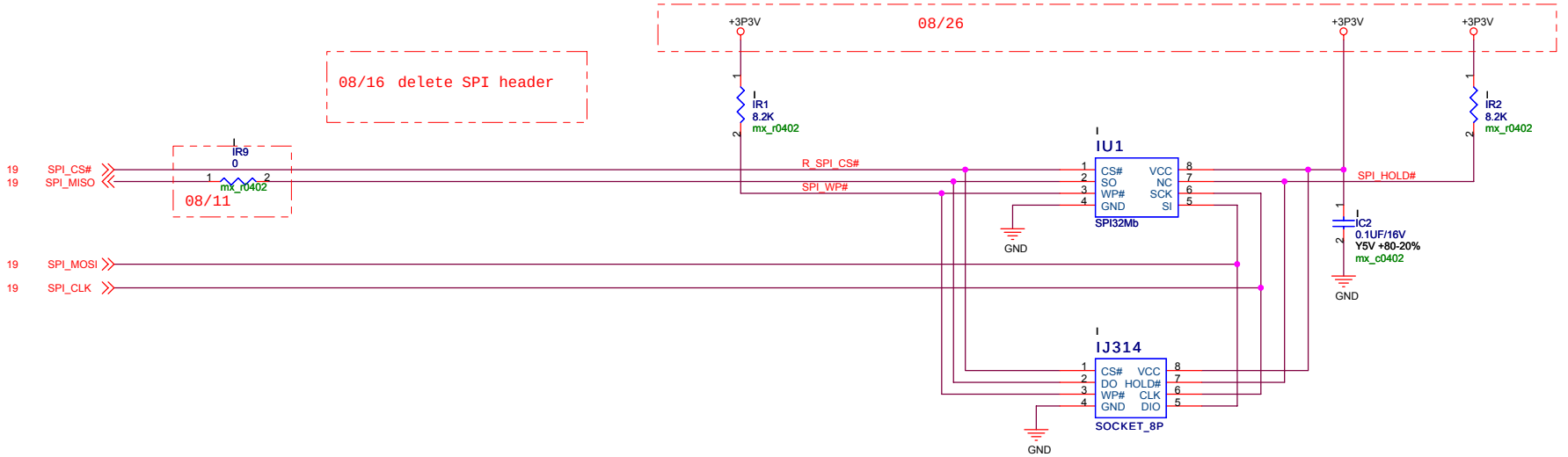


PEGATRON	Title : FRONT PANEL CIRCUIT	
Pegatron Corp.	Engineer: Livy_Zhu	
Size: A3	Project Name: IPMSB-BE/CR	Rev: 1.00
Date: Friday, September 24, 2010	Sheet 58 of 83	

SM BUS Control

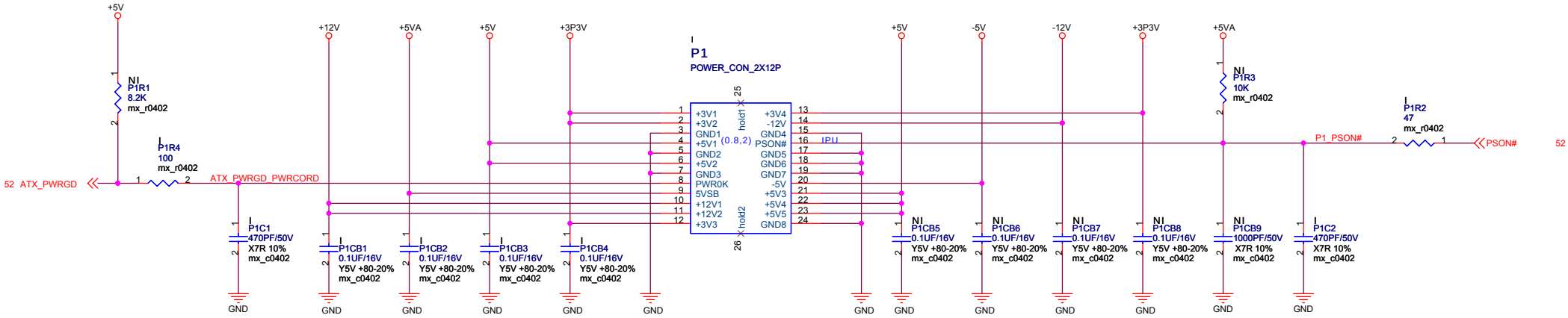


SPI BIOS ROM - 32 Mbit

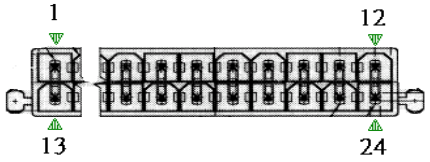


PEGATRON	Title : SPI ROM	
Pegatron Corp.	Engineer: Livy_Zhu	
Size: A3	Project Name: IPMSB-BE/CR	Rev: 1.00
Date: Friday, September 24, 2010	Sheet 59 of 83	

ATX POWER_24P SUPPLY CONNECTOR



BOTTOM SIDE VIEW



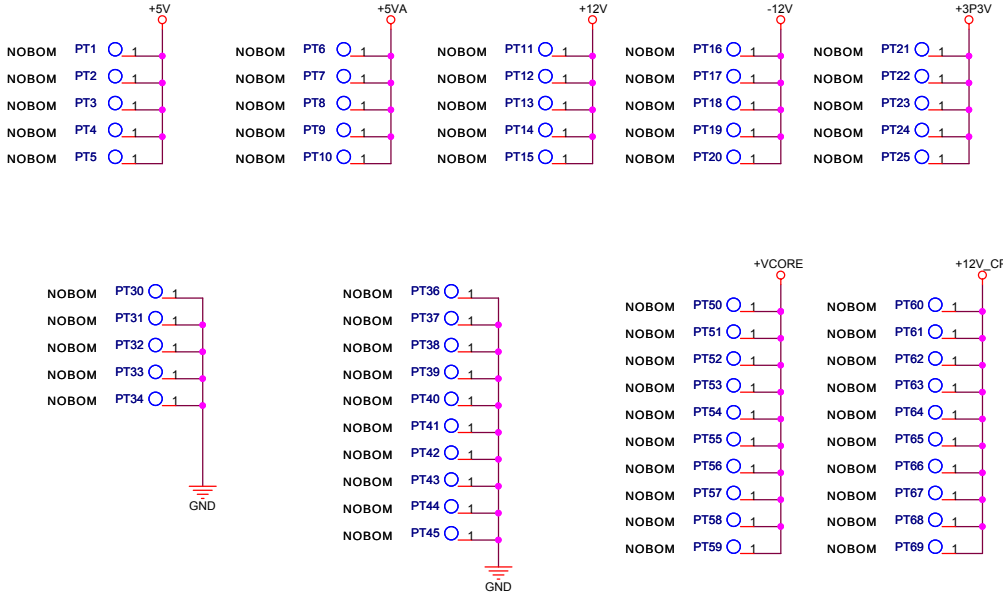
TOP SIDE VIEW

PCB

IPM61-BE R1.00

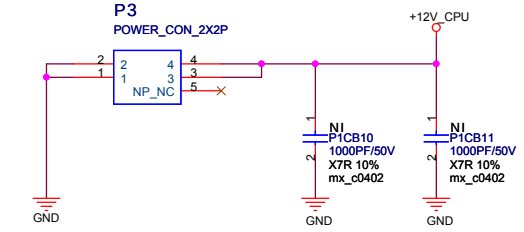
08X000000000

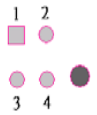
VRM POWER_4P SUPPLY CONNECTOR



Nodes related to different power planes

Node	Goal Q'ty
+5V	5
+5VSB	5
+12V	5
-12V	5
+3V	5
+Vcore	10
GND	15
+12V_CPU	10





BOTTOM SIDE VIEW

PEGATRON Title : ATX 24P CONN

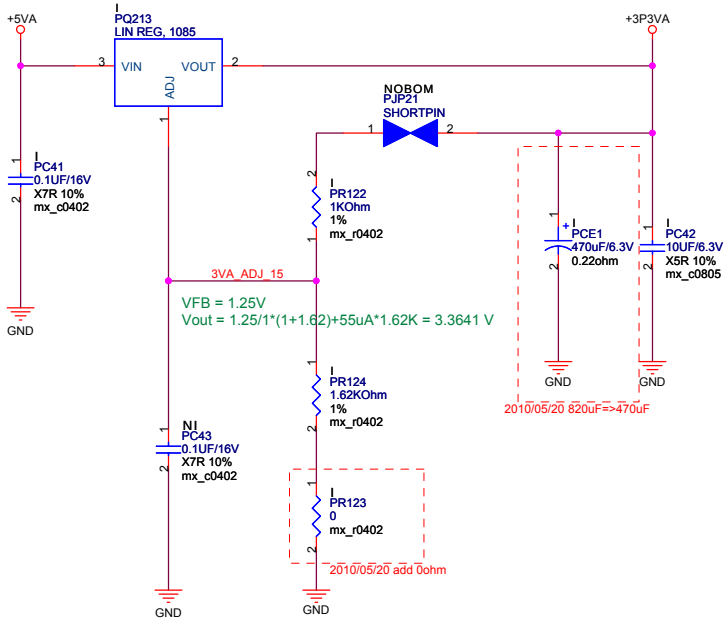
Pegatron Corp. Engineer: Livy_Zhu

Size	Project Name	Rev
A3	IPMSB-BE/CR	1.00

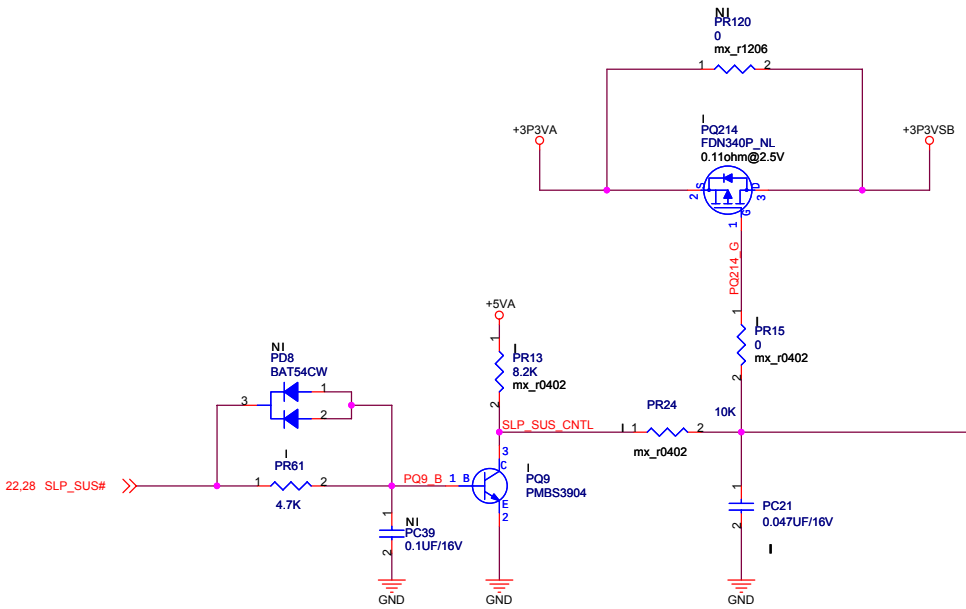
Date: Friday, September 24, 2010 Sheet 60 of 83

+3P3VA

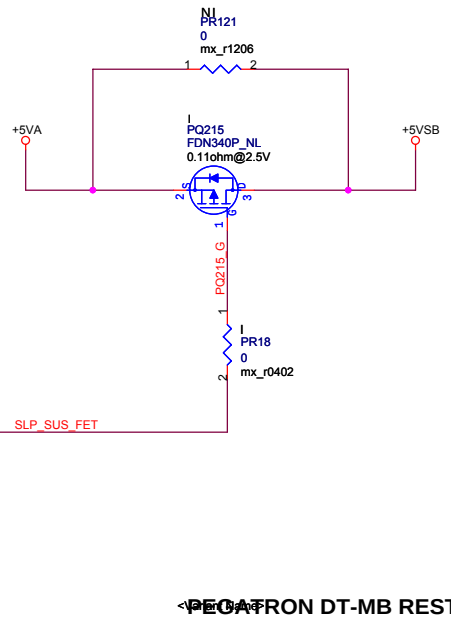
Imax = 1.5A
Pd = 2.55W



+3P3VA => +3VSB



+5VA => +5VSB

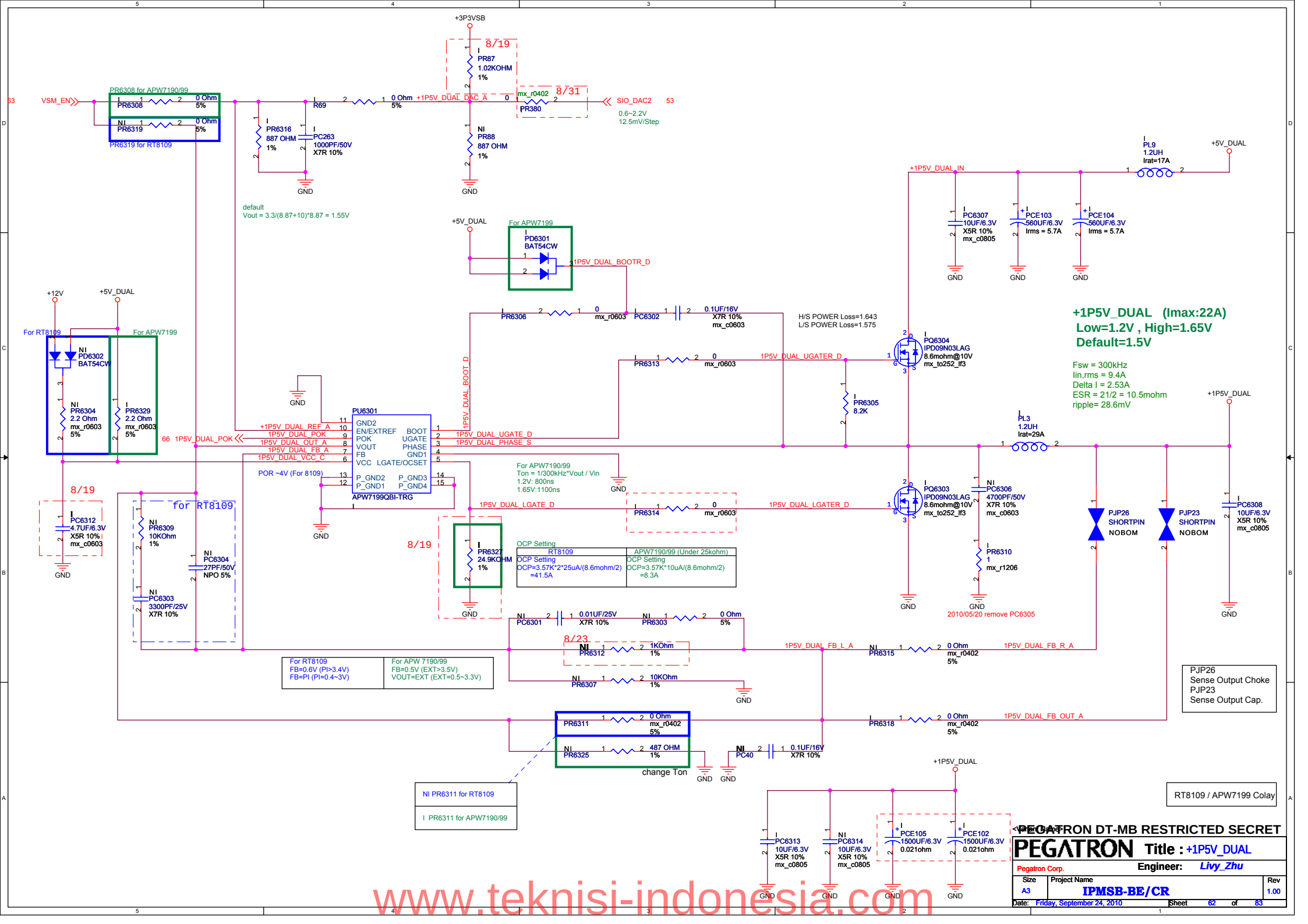


PEGATRON Title : +3VA,+3VSB,+5VSB

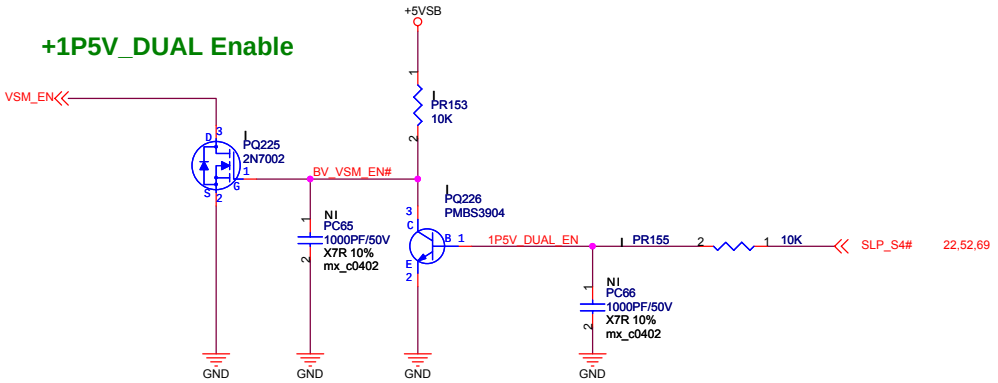
Pegatron Corp. Engineer: Livy_Zhu

Size	Project Name	Rev
A3	IPMSB-BE/CR	1.00

Date: Friday, September 24, 2010 Sheet 61 of 83

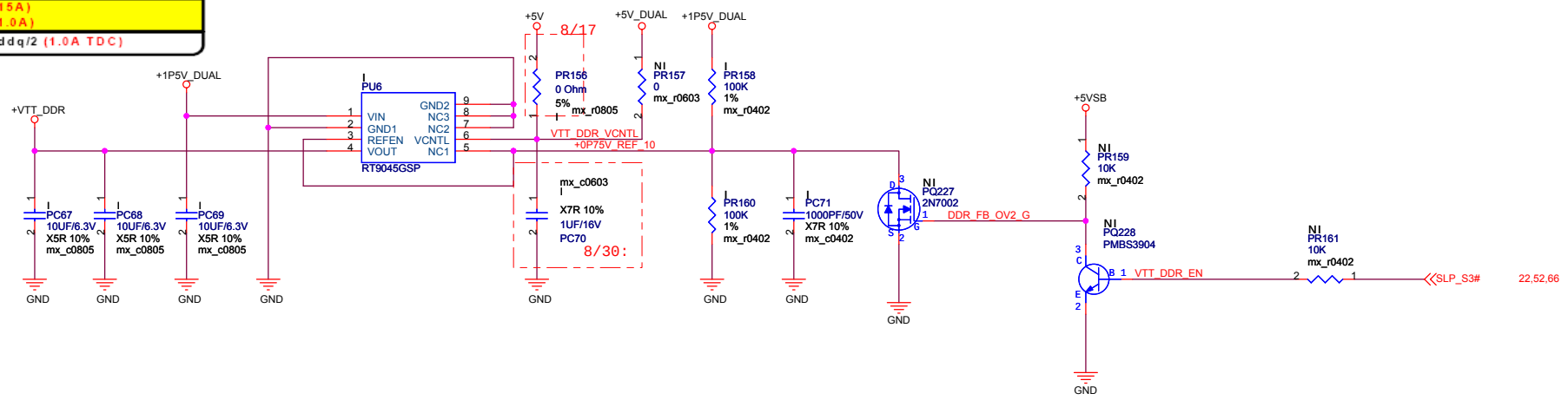


+1P5V_DUAL Enable



+1P5V_DUAL ==> +VTT_DDR...(1A)

DDR3 DIMM (4) 1333MHz
V_SM$_{80}$: Vddq (1.5A)
V_SM$_{83}$: Vddq (1.0A)
V_SM_VTT$_{80}$: Vddq/2 (1.0A TDC)

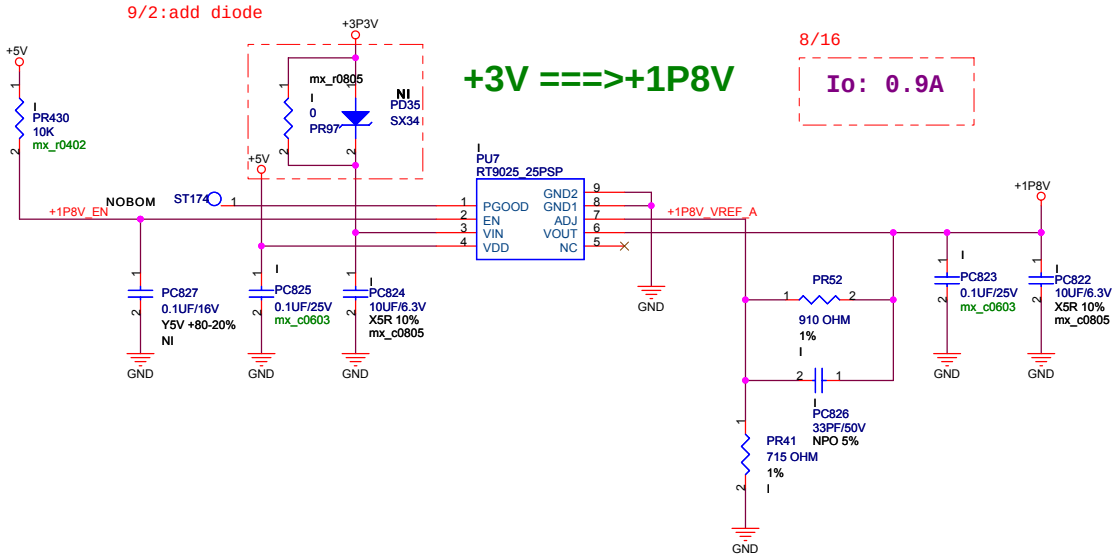


PEGATRON Title : +VTT_DDR&+1P5V_DUAL_EN

Pegatron Corp. Engineer: Livy_Zhu

Size	Project Name	Rev
A3	IPMSB-BE/CR	1.00

Date: Friday, September 24, 2010 Sheet 63 of 83



PEGATRON Title : +1P8V FOR SATA3.0

Pegatron Corp. Engineer: Livy_Zhu

Size	Project Name	Rev
A3	IPMSB-BE/CR	1.00

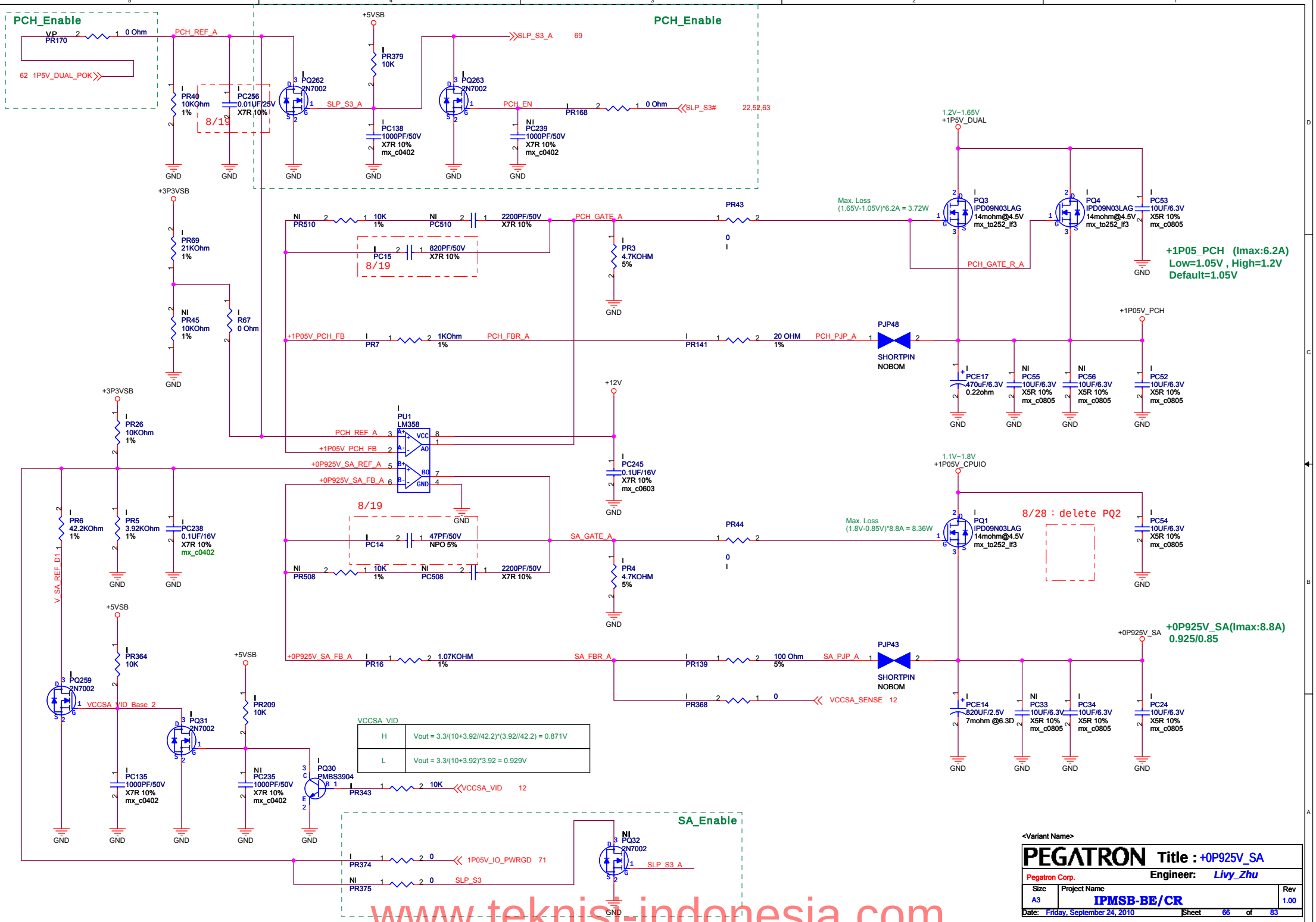
Date: Friday, September 24, 2010 Sheet 64 of 83

PEGATRON Title : VSA_OV_FUNCTION

Pegatron Corp. Engineer: Livy_Zhu

Size	Project Name	Rev
A3	IPMSB-BE/CR	1.00

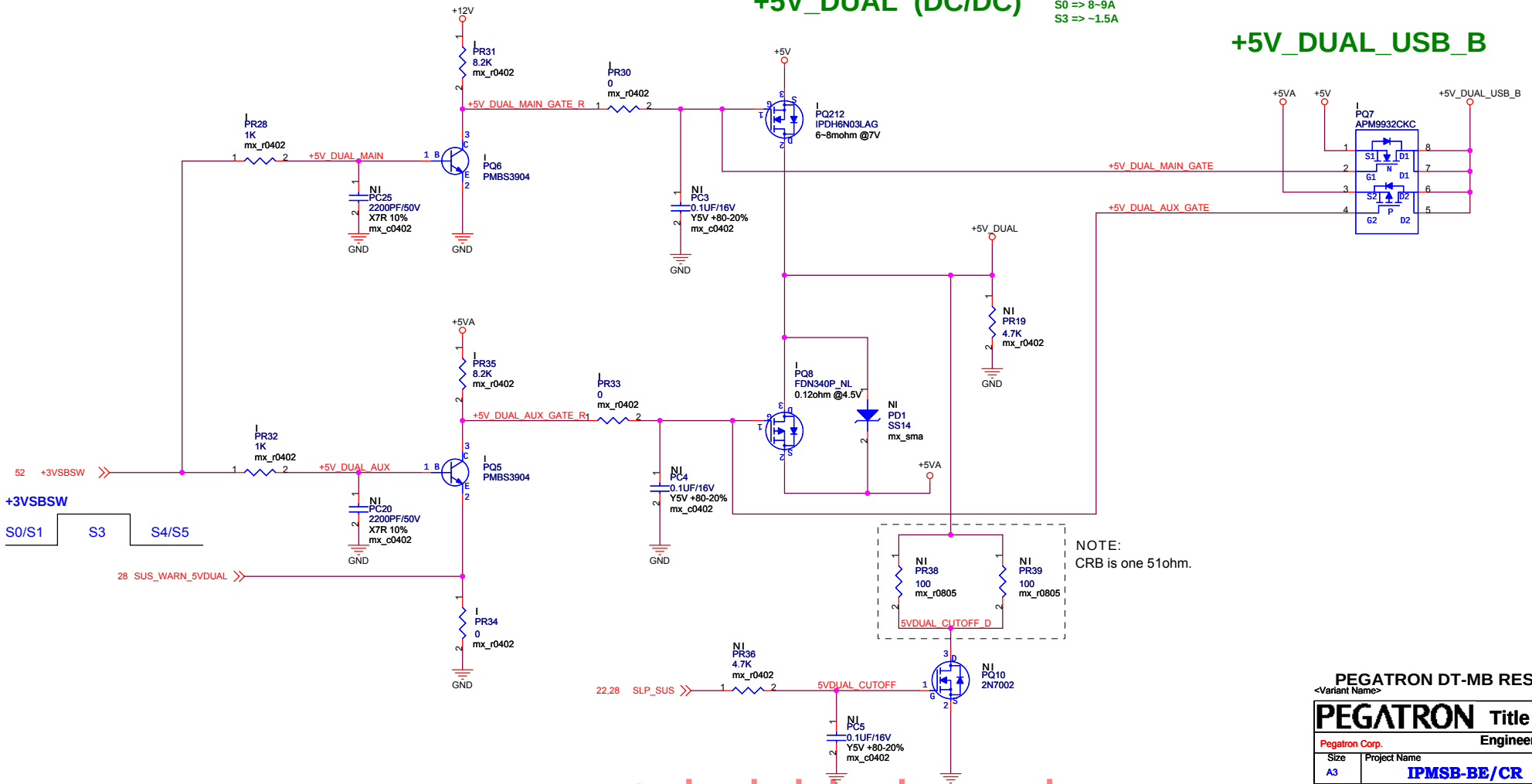
Date: Friday, September 24, 2010 Sheet 65 of 83



+5V_DUAL (DC/DC)

+5V_DUAL
S0 => 8~9A
S3 => ~1.5A

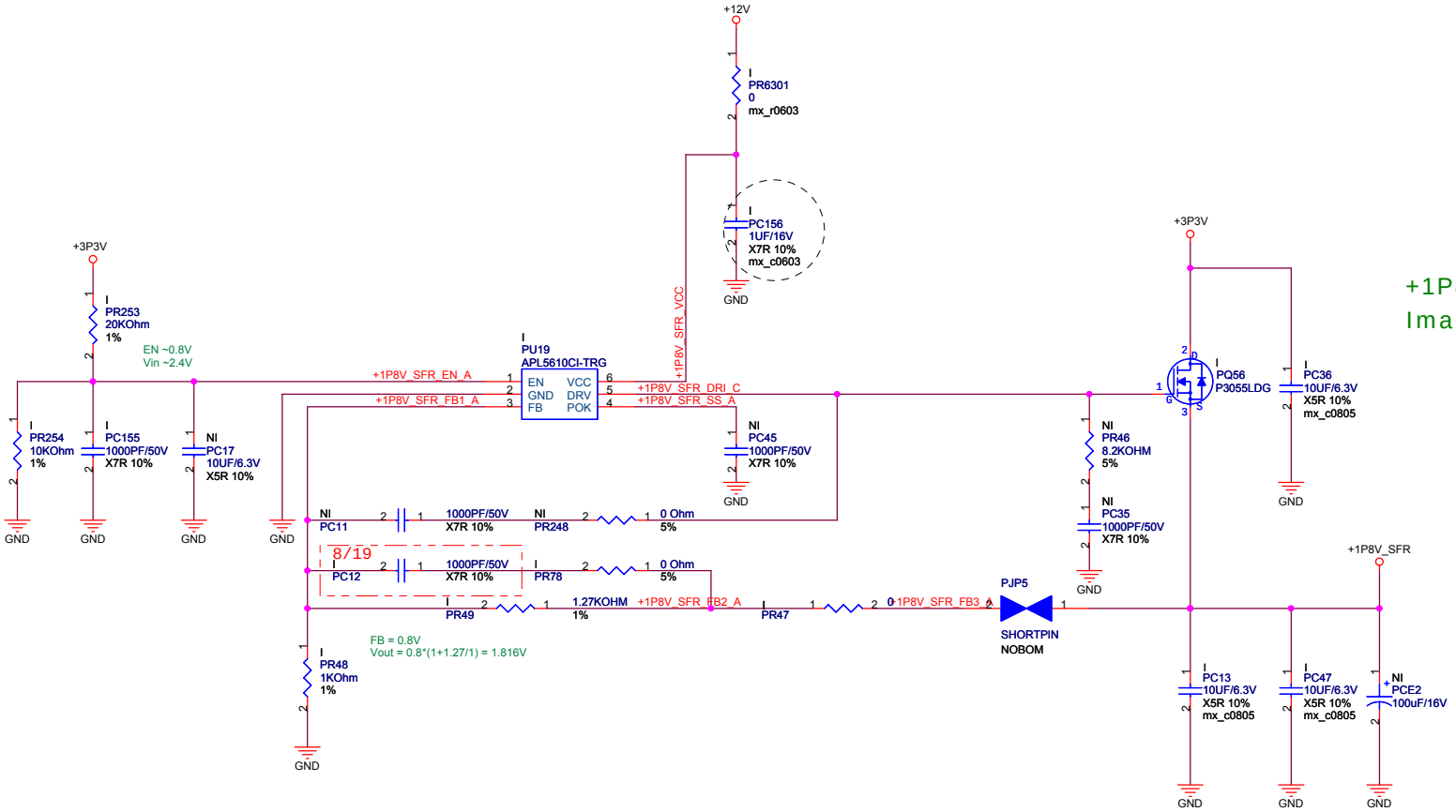
+5V_DUAL_USB_B



PEGATRON DT-MB RESTRICTED SECRET

<Variant Name>

PEGATRON	Title : DUAL POWER	
Pegatron Corp.	Engineer: Livy_Zhu	
Size: A3	Project Name: IPMSB-BE/CR	Rev: 1.00
Date: Friday, September 24, 2010	Sheet 67 of 83	

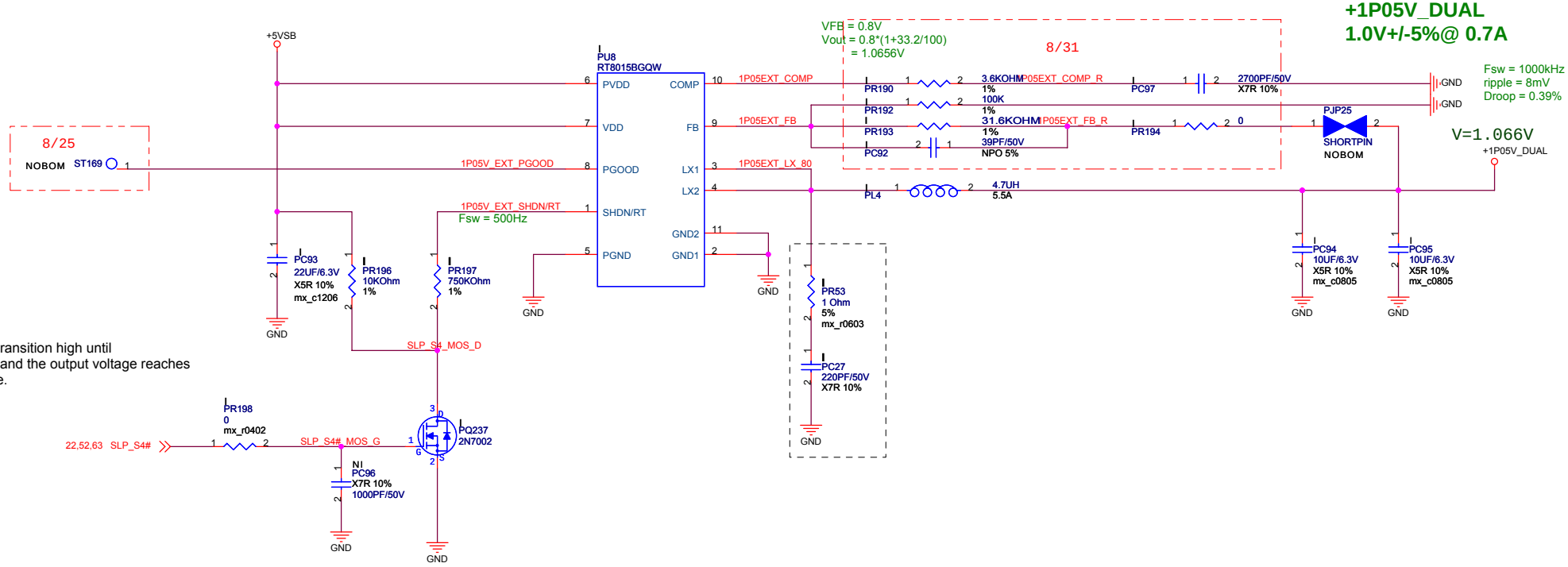


PEGATRON Title : +1P8V_SFR

Pegatron Corp. Engineer: Livy_Zhu

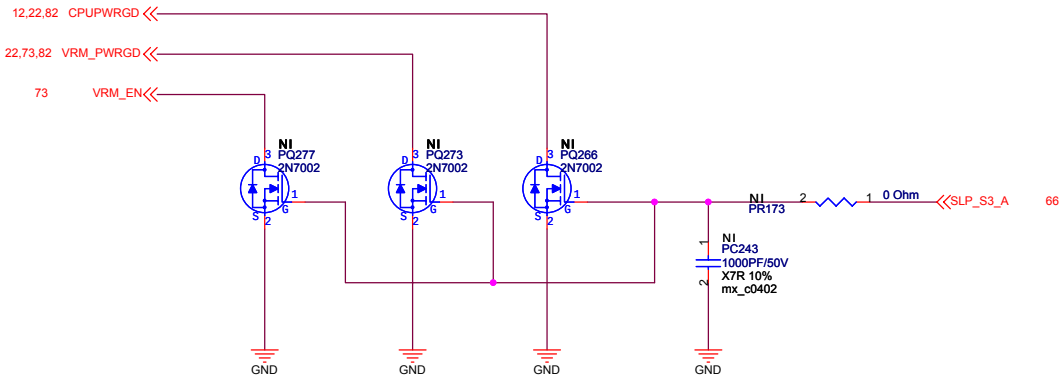
Size	Project Name	Rev
A3	IPMSB-BE/CR	1.00

Date: Friday, September 24, 2010 Sheet 68 of 83



NOTE:
PGOOD is allowed to transition high until soft start finished over and the output voltage reaches 87.5% of its set voltage.

VRM_EN

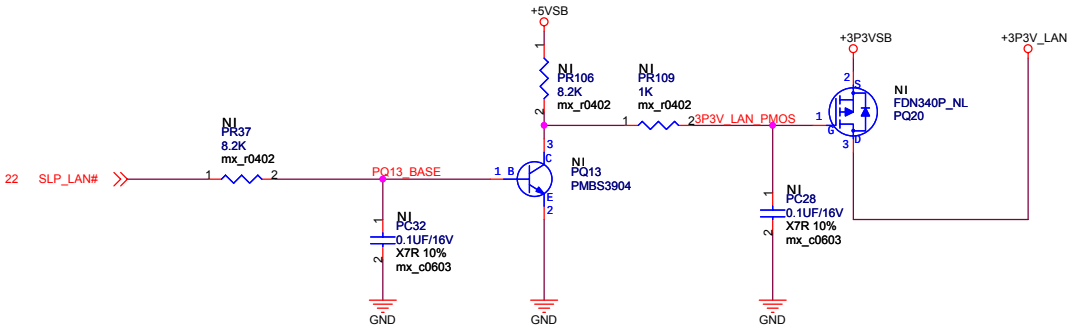


PEGATRON Title : +1V_DUAL

Pegatron Corp. Engineer: Livy_Zhu

Size	Project Name	Rev
A3	IPMSB-BE/CR	1.00

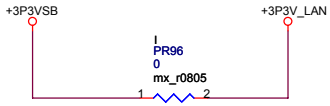
Date: Friday, September 24, 2010 Sheet 69 of 83



Lewisville (LAN)

V3.3S_LAN (0.218A) (ODSVR)

V1.0S_LAN (332mA)



+3P3V_LAN

8/26:delete +3P3V_ME

PEGATRON Title : +3P3V_LAN +3P3V_ME

Pegatron Corp. Engineer: Livy_Zhu

Size	Project Name	Rev
A3	IPMSB-BE/CR	1.00

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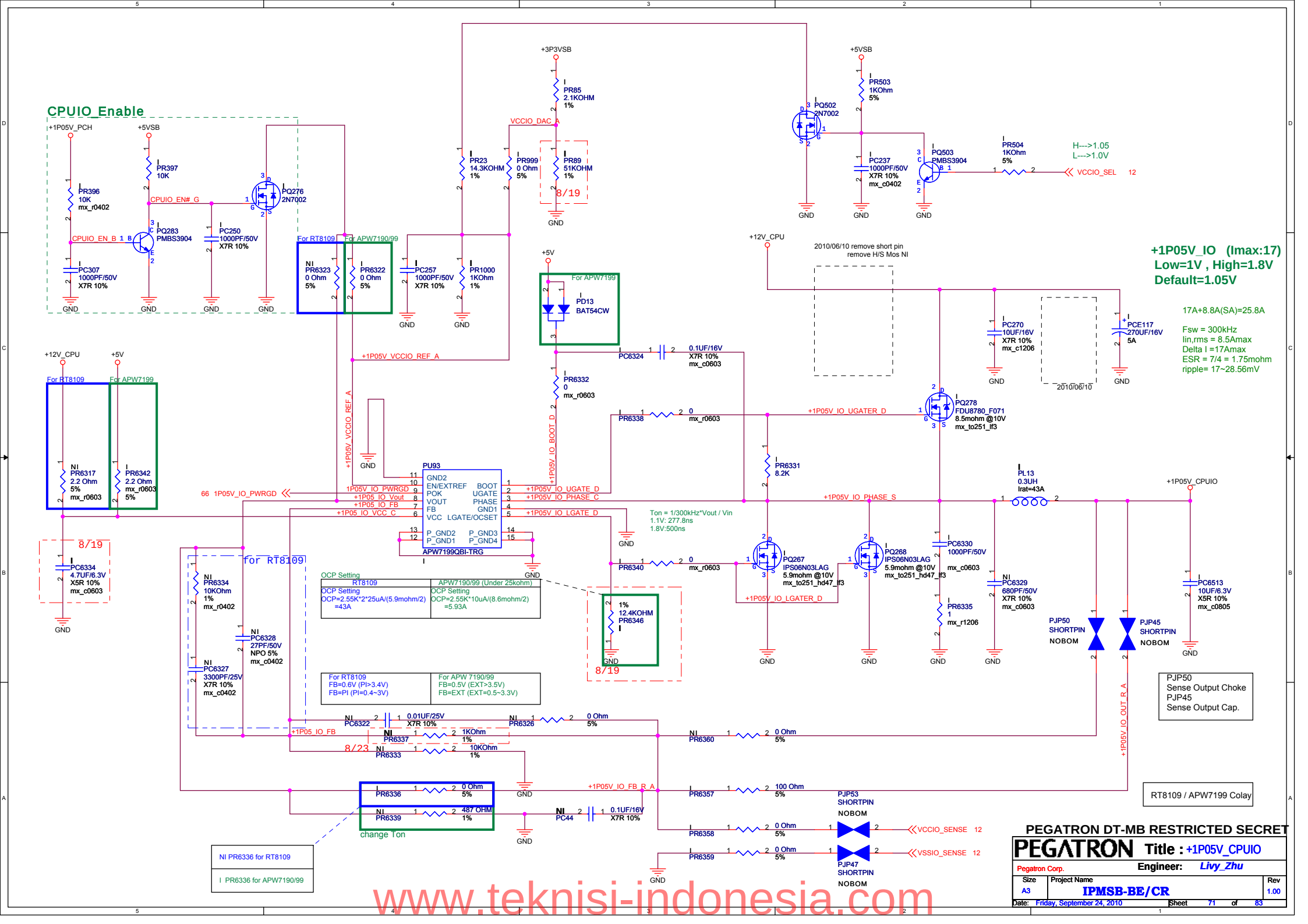
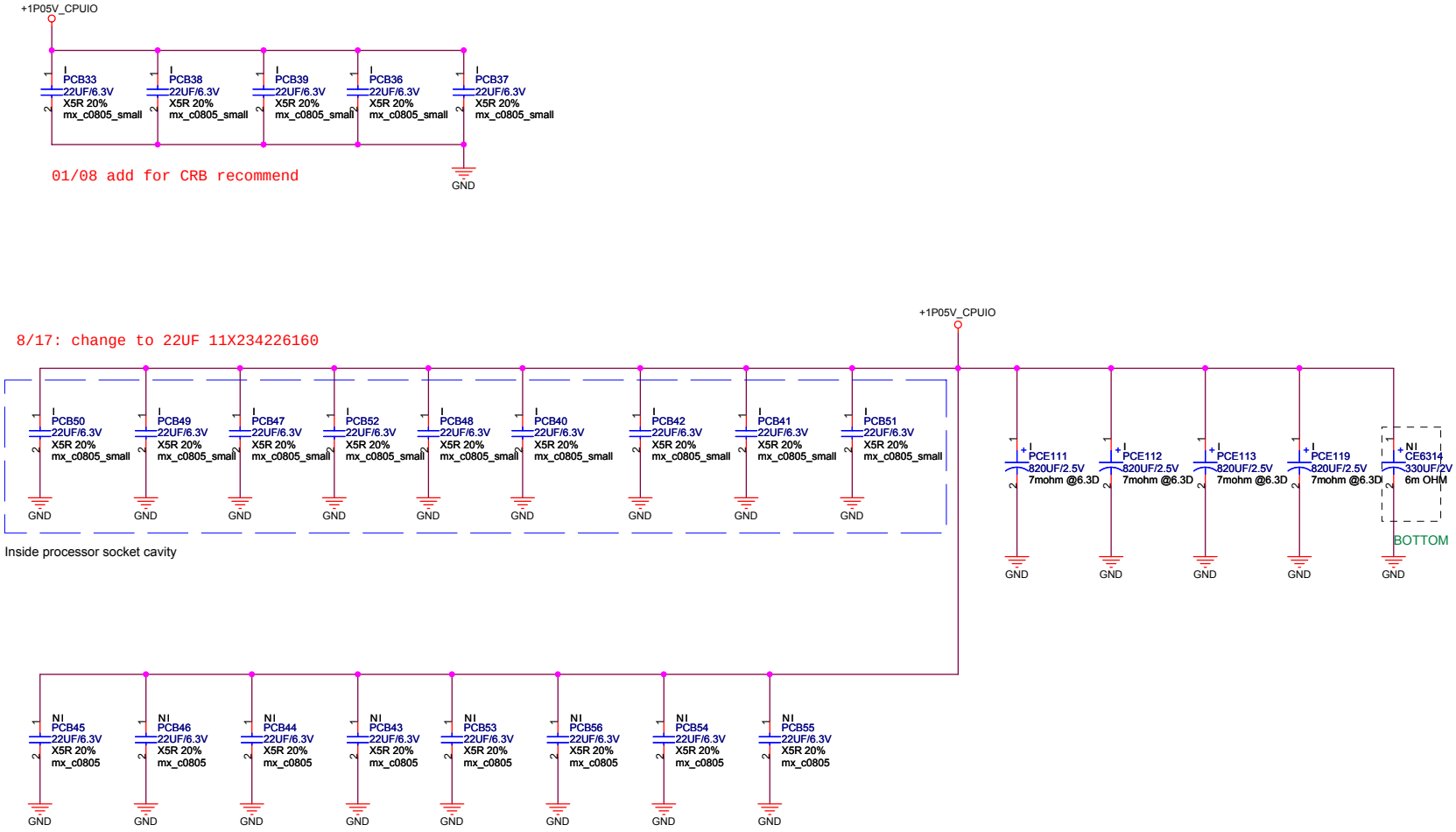

CPUIO_Enable
+1P05V_IO (Imax:17)
Low=1V , High=1.8V
Default=1.05V
17A+8.8A(SA)=25.8A
Fsw = 300kHz
Iin,rms = 8.5Amax
Delta I =17Amax
ESR = 7/4 = 1.75mohm
ripple= 17~28.56mV
2010/06/10 remove short pin
remove H/S Mos NI
PU93
APW7199QBI-TRG
PJP50
Sense Output Choke
PJP45
Sense Output Cap.
RT8109 / APW7199 Colay
PEGATRON DT-MB RESTRICTED SECRET
PEGATRON Title : +1P05V_CPUIO
Pegatron Corp. Engineer: Livy_Zhu
Size A3 Project Name IPMSB-BE/CR Rev 1.00
Date: Friday, September 24, 2010 Sheet 71 of 83
www.teknisi-indonesia.com

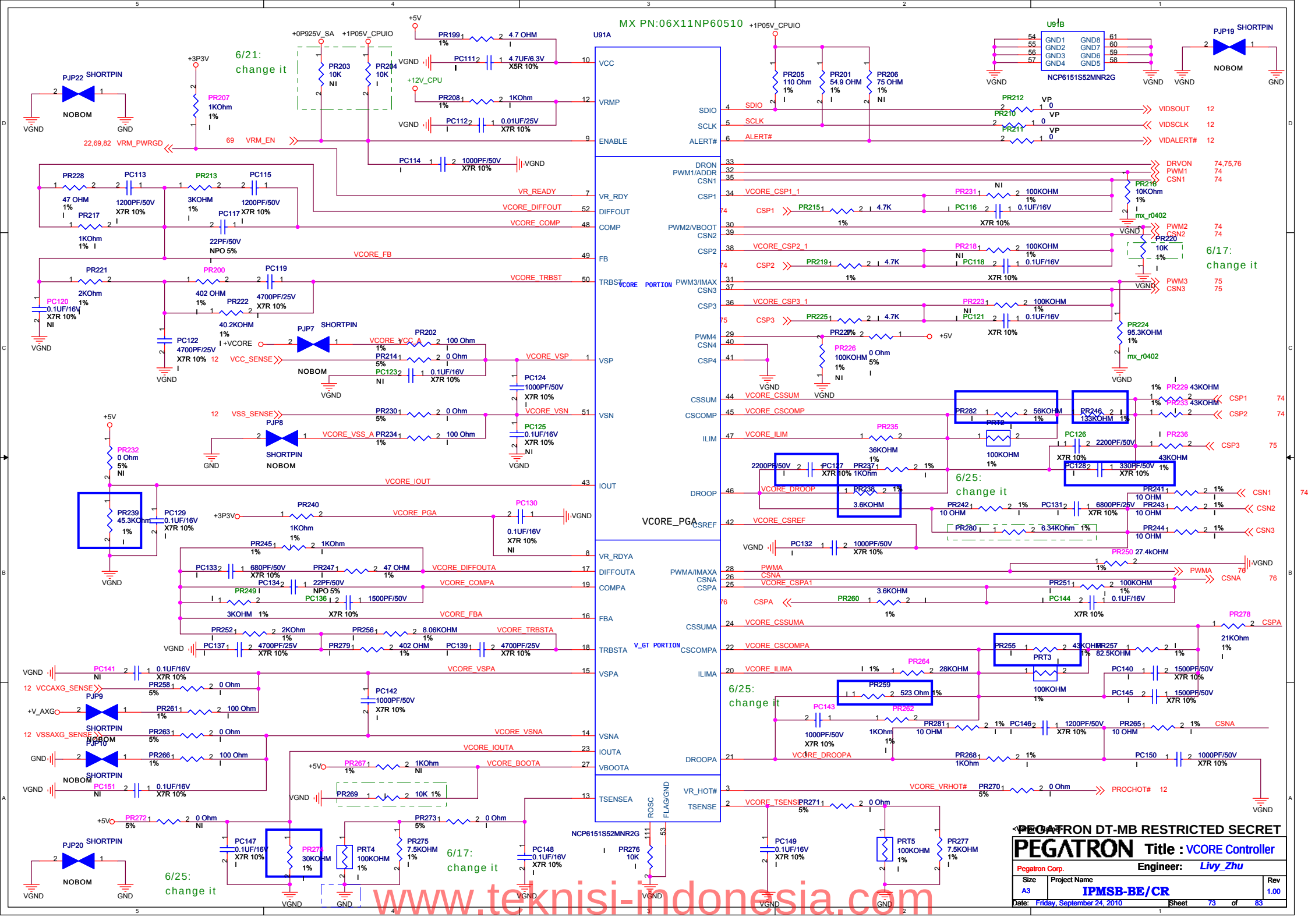


PEGATRON Title : +1P05V_CPUIO CAP

Pegatron Corp. Engineer: Livy_Zhu

Size	Project Name	Rev
A3	IPMSB-BE/CR	1.00

Date: Friday, September 24, 2010 Sheet 72 of 83



PEGATRON Title : VCORE Controller

Pegatron Corp. Engineer: Livy_Zhu

Size	Project Name	Rev
A3	IPMSB-BE/CR	1.00

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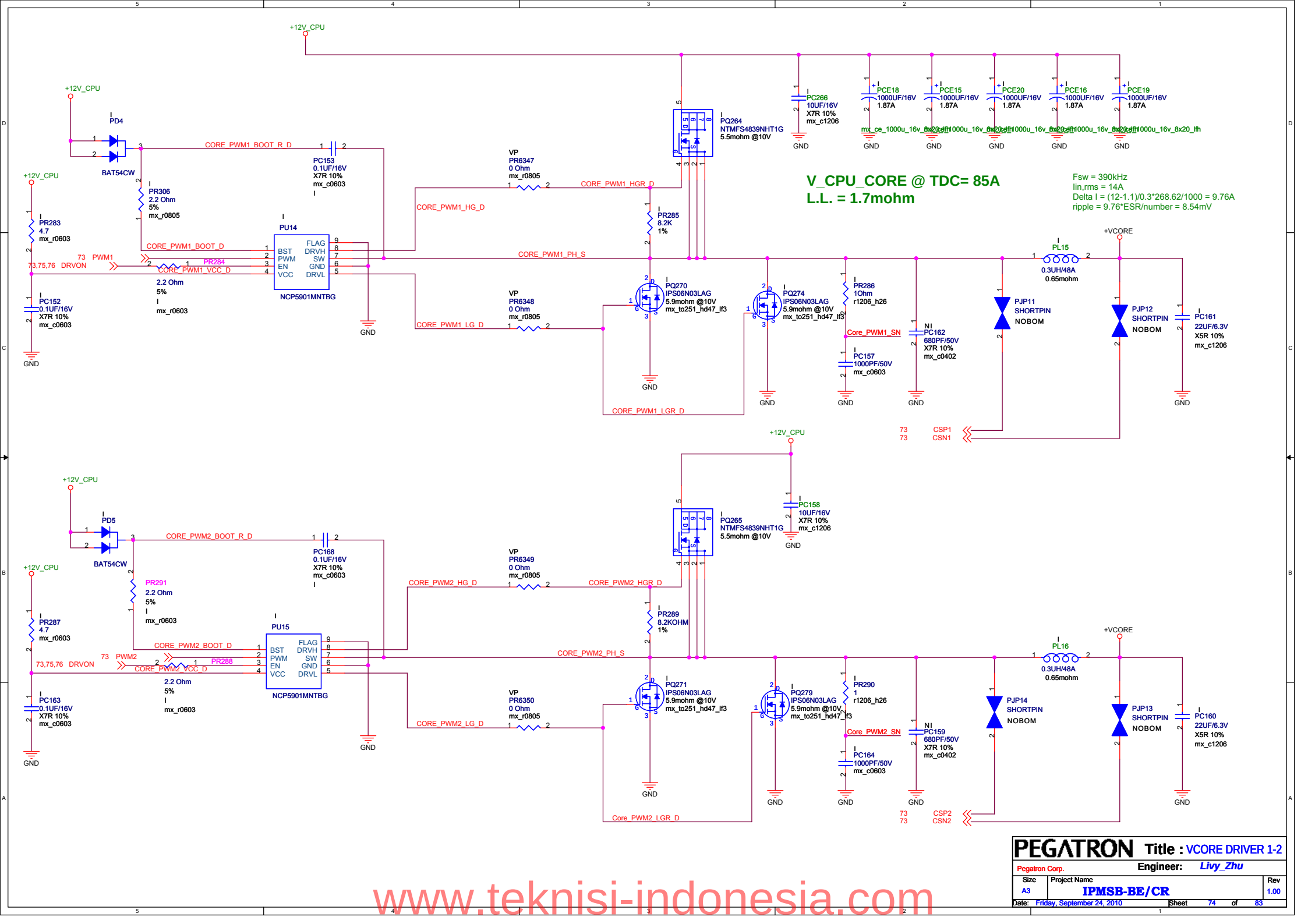
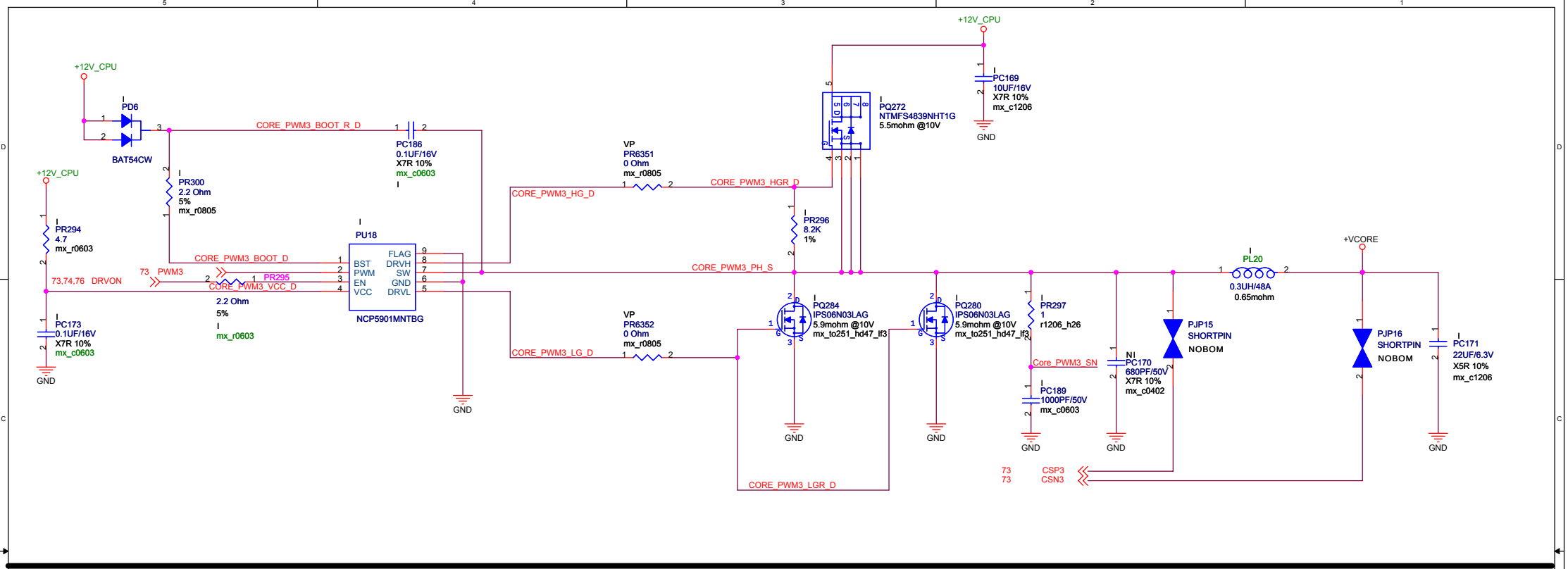


PEGATRON	Title : VCORE DRIVER 1-2	
Pegatron Corp.	Engineer: Livy_Zhu	
Size: A3	Project Name: IPMSB-BE/CR	Rev: 1.00
Date: Friday, September 24, 2010	Sheet 74 of 83	

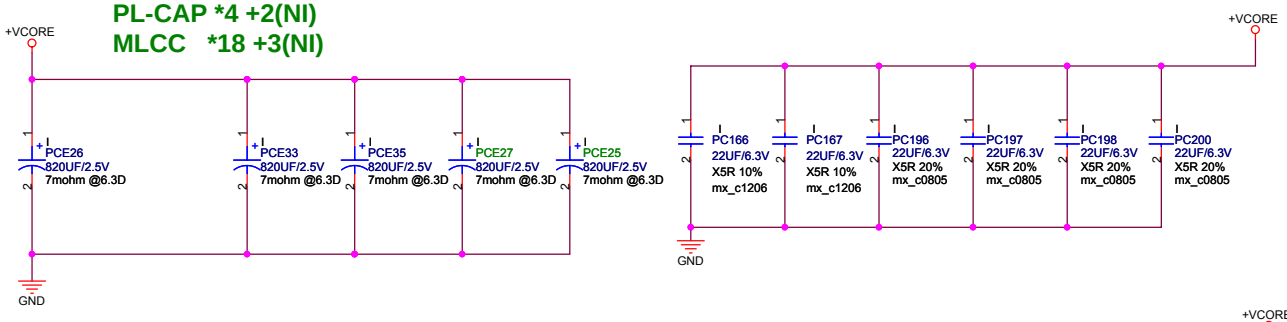


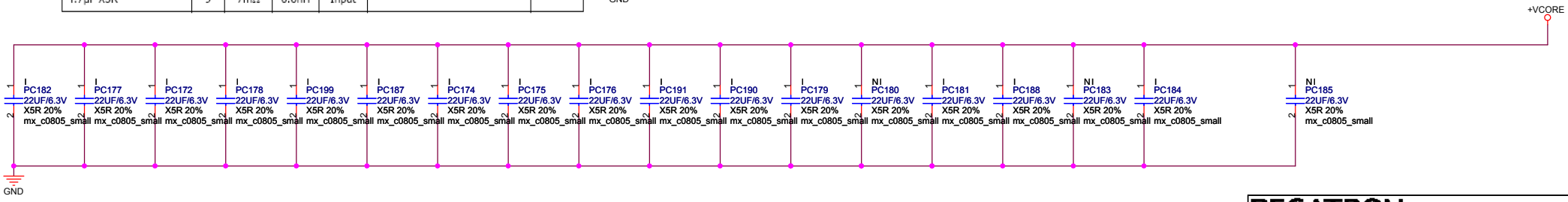
Output CAP

Table 30-2. Decoupling Requirements

Capacitance	Qty	ESR (each)	ESL (each)	Filter	Placement	Notes
Aluminum Polymer 560µF	4	7mΩ	1.4nH	Output	North of processor - as close to RM keep-out as possible	1
22µF 0805 X5R	18	5mΩ	0.55nH	Output	14 - Inside processor socket cavity 4- North of processor - as close to RM keep-out as possible	1, 2 3
Aluminum Electrolytic 390µF	4	51mΩ	6.1nH	Input		1
4.7µF X5R	9	7mΩ	0.6nH	Input		1

PL-CAP *4 +2(NI)
MLCC *18 +3(NI)





PEGATRON Title : VCORE DRIVER 2-2

Pegatron Corp. Engineer: Livy_Zhu

Size	Project Name	Rev
A3	IPMSB-BE/CR	1.00

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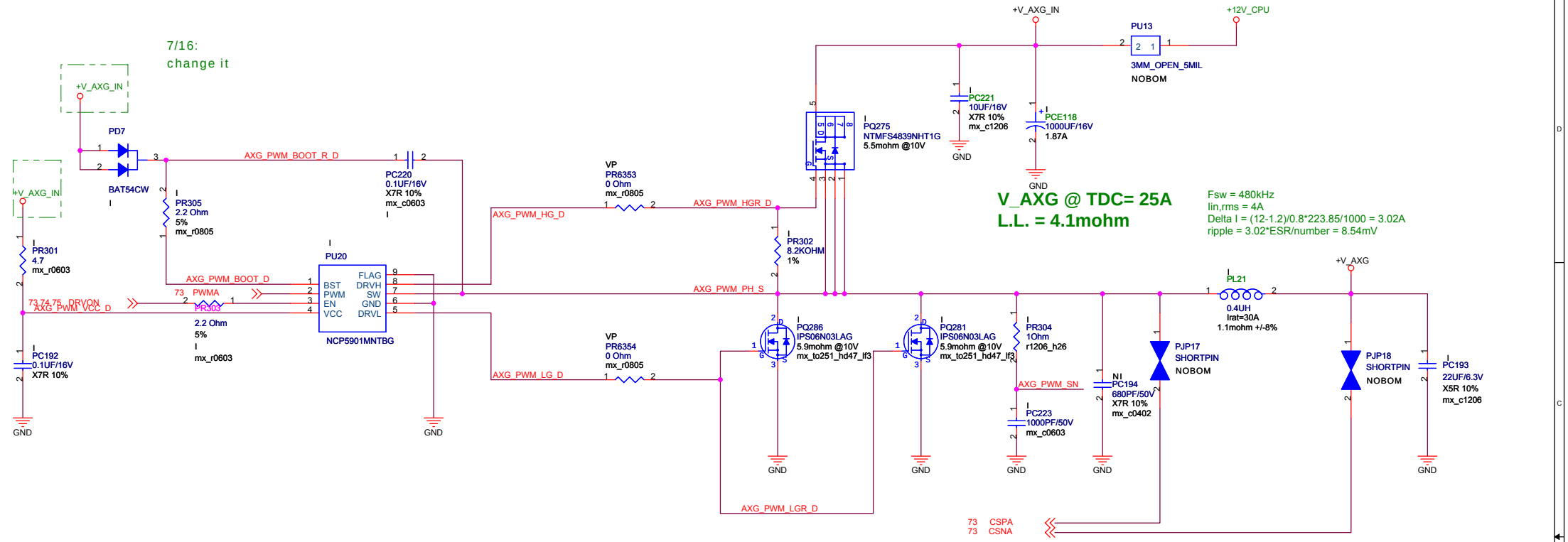
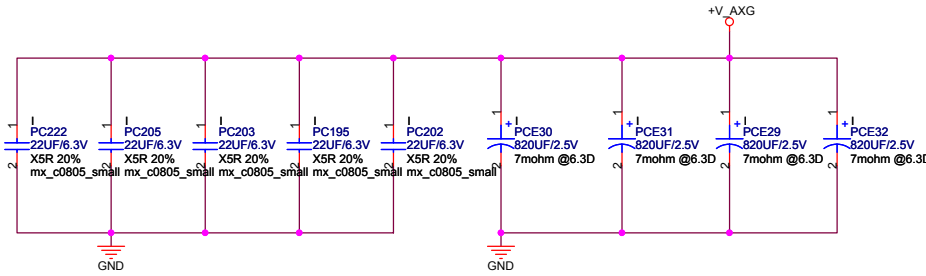


Output CAP

Table 30-4. VCCAXG Decoupling Requirements

Capacitance	Qty	ESR (each)	ESL (each)	Filter	Placement	Notes
Aluminum Polymer 560µF	4	7mΩ	1.4nH	Output	East of processor - as close to RM keep-out as possible	1
22µF 0805 X5R	6	5mΩ	0.55nH	Output	4 - inside processor socket cavity 2(empty) - Bottom of board, near socket	1, 2 3
4.7µF X5R	3	7mΩ	0.6nH	Input		1

PL-CAP *4
MLCC *6



PEGATRON Title : +VAXG_DRIVER

Pegatron Corp. Engineer: Livy_Zhu

Size	Project Name	Rev
A3	IPMSB-BE/CR	1.00

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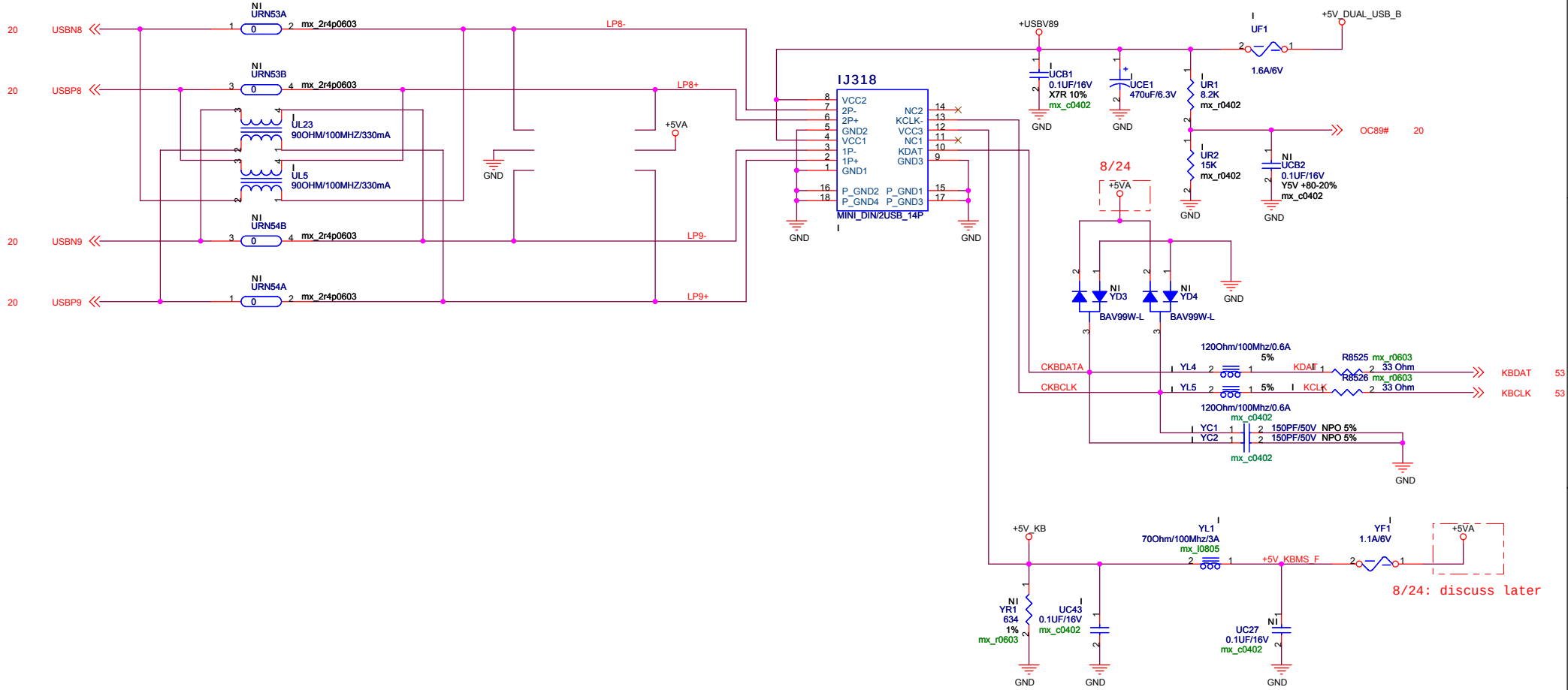
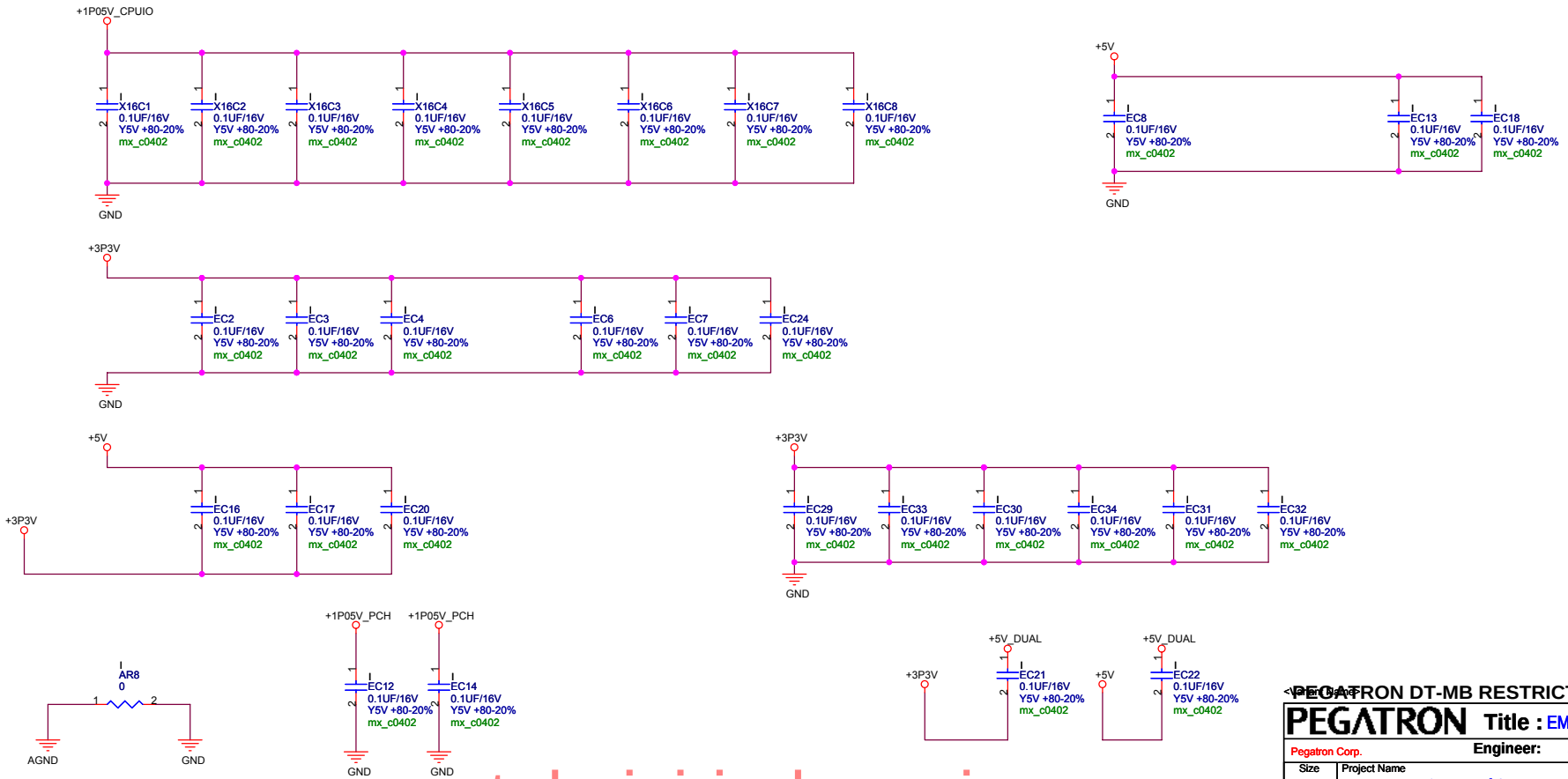
Back PS/2 with dual USB connector



PEGATRON	Title : PS2+USB CONN	
Pegatron Corp.	Engineer: Livy_Zhu	
Size: A3	Project Name: IPMSB-BE/CR	Rev: 1.00
Date: Friday, September 24, 2010	Sheet 77 of 83	



PEGATRON Title : EMI CAP

Pegatron Corp. Engineer: Livy_Zhu

Size	Project Name	Rev
A3	IPMSB-BE/CR	1.00

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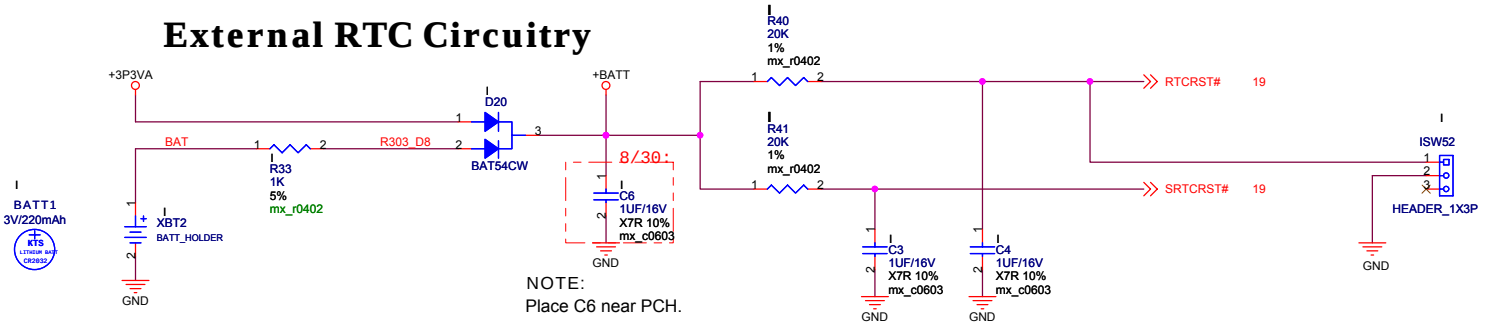
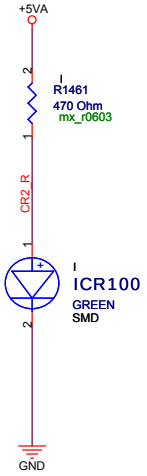
External RTC Circuitry



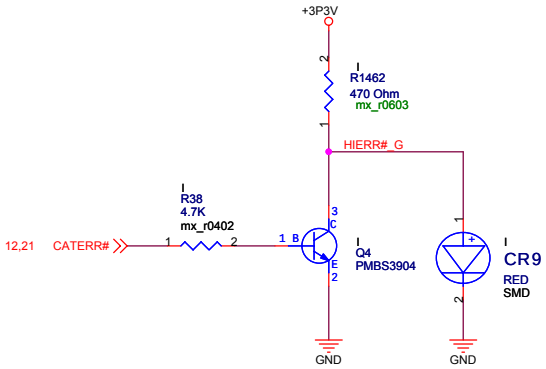
NOTE:
Place C6 near PCH.

Battery Socket

Standby LED

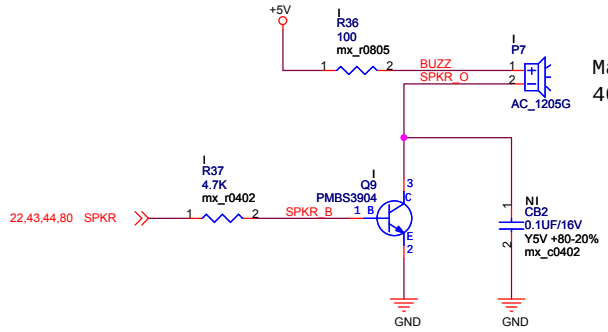


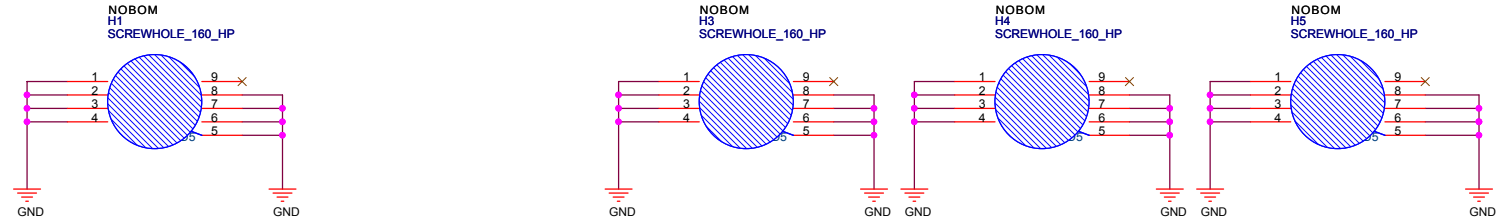
IERR# : RED



SPEAKER

I=5/(100+40)=35.7mA





ONLY FOR INTEL SCREW HOLE

LB1
1.375X0.25
WHITE
1D375X0D25_WHITE

LB2
1.0X0.187
WHITE
1D0X0D187_WHITE

AA# : 1510-03MQ0IN (S : 1510-03MR0IN)

Product code : 1510-06DE0IN

LB4
8/12 DIP
1.0X0.187
WHITE
1D0X0D187_WHITE

Product code : 1510-06DE0IN

PEGATRON Title : RTC/CMOS/SPKR

Pegatron Corp. Engineer: Livy_Zhu

Size	Project Name	Rev
A3	IPMSB-BE/CR	1.00

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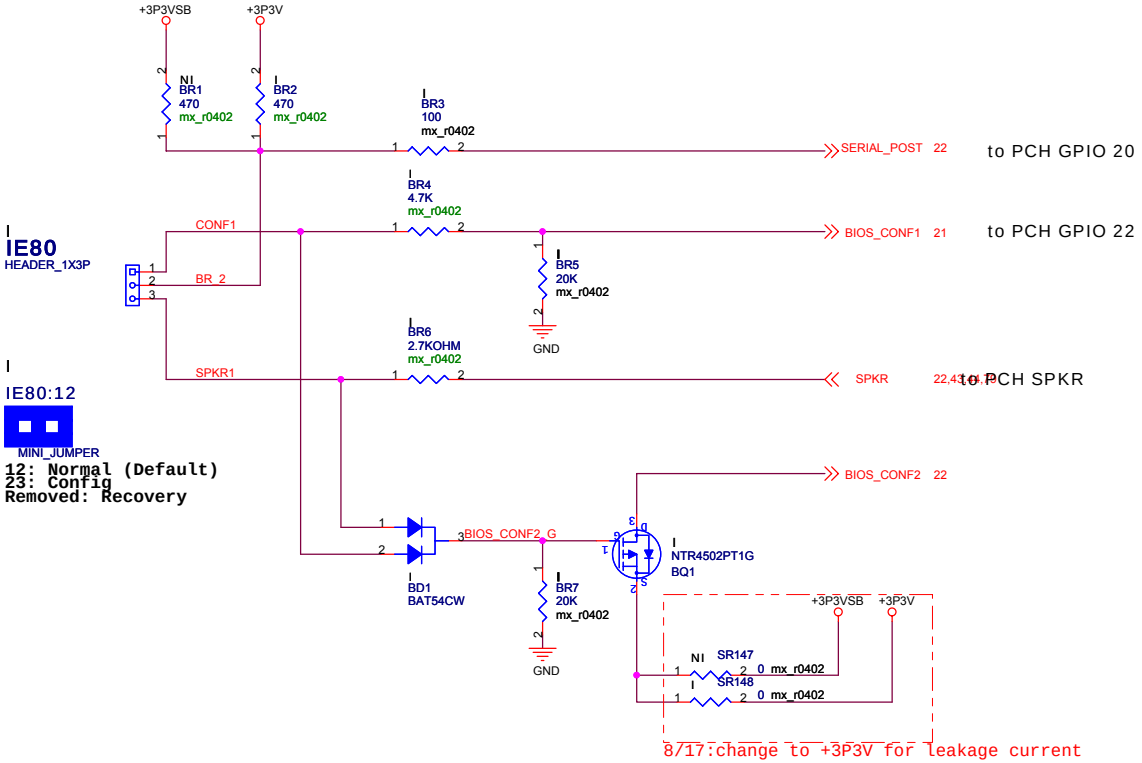
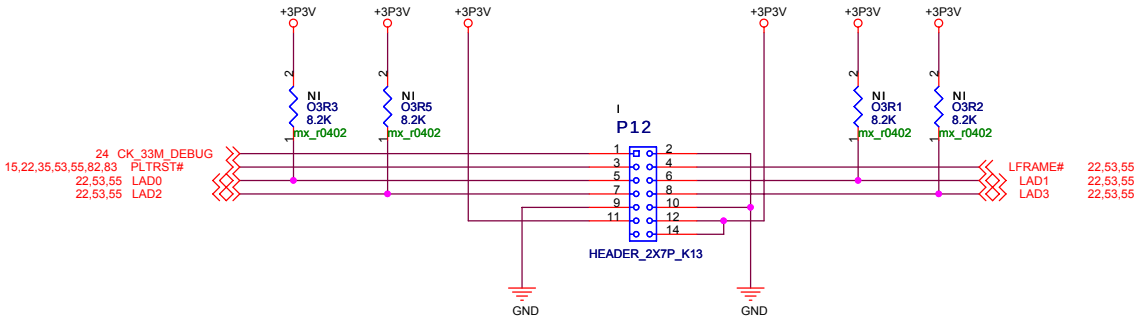
BIOS CONFIGURATION



LPC DEBUG PORT

08/13: NI LPC From Fab.B
(after PCI debug verified)



PEGATRON Title : BIOS and LPC header

Pegatron Corp. Engineer: Livy_Zhu

Size	Project Name	Rev
A3	IPMSB-BE/CR	1.00

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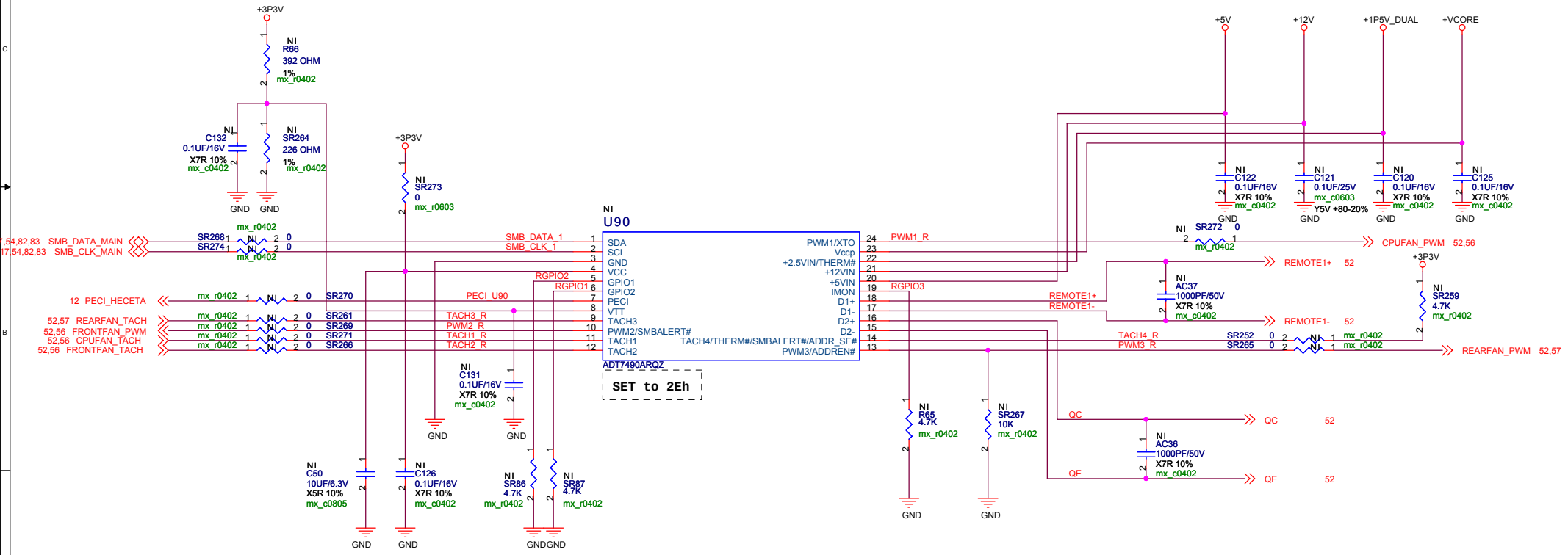

PEGATRON Title : Heceta Fan Control

Pegatron Corp. Engineer: Livy_Zhu

Size	Project Name	Rev
A3	IPMSB-BE/CR	1.00

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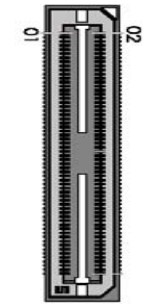
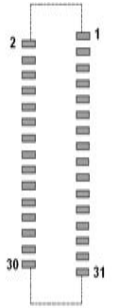
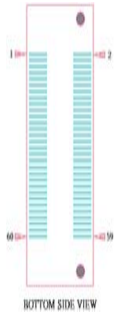


TOP SIDE VIEW



HRS/DF9C-31S-1V(22)
PCB FOOTPRINT



BOTTOM SIDE VIEW

INTEL CPU XDP DEBUG PORT

NOTE:
CRB is BTM

NOTE:
Please close to each other to reduse stub.

NOTE:
Place HR64 near HR24, reduce stub

XDP1
BtoB_CON_60P

+1P05V_CPUIO
HCB20 0.1UF/16V Y5V +80-20% mx_c0402
GND

VCC_OBS_AB
VCC_OBS_CD

TCK1 TCK0 TDO TRSTn TDI TMS
TCK 12
TDO 12
TRST# 12
TDI 12
TMS 12

HOOK0 CPUXDP_HOOK0
HR61 1.5K mx_r0402 (NI)
HR62 249 1% mx_r0402
CPUPWRGD 12,22,69

HR63 1K mx_r0402 (NI)

HOOK1 CPUXDP_HOOK1
HOOK2 CPUXDP_HOOK2
HOOK3 CPUXDP_HOOK3
HOOK6/RESET#
HOOK7/DBR#
HR65 1K mx_r0402 (NI) PLTRST# 15,22,35,53,55,80,83
HR66 3.3K mx_r0402 PWRBTN# 52,58
HR64 1K mx_r0402 CPU_CFG0 12
HR67 0 mx_r0402 VRM_PWRGD 22,69,73
CPURST_XDP# 15,83
SYS_RESET_DBR# 12,22,83

SC43 0.1UF/16V X7R 10% (NI)
GND

H_PREQ# H_PRDY# BPM0# BPM1# BPM2# BPM3#
OBSFN_A0 OBSFN_A1 OBSDATA_A0 OBSDATA_A1 OBSDATA_A2 OBSDATA_A3
BPM4# BPM5# BPM6# BPM7#
OBSFN_B0 OBSFN_B1 OBSDATA_B0 OBSDATA_B1 OBSDATA_B2 OBSDATA_B3

24 CK_100M_CPUXDP
24 CK_100M_CPUXDP#
HR68 HR69 mx_r0402
CPU_XDPCLK CPU_XDPCLK#
HR72 HR73 mx_r0402
CPU_ITPCLK_HOOK4 CPU_ITPCLK# HOOK5
ITPCLK/HOOK4 ITPCLK#/HOOK5

12 CK_100M_CPU_XDP
12 CK_100M_CPU_XDP#
HR74 HR75 (NI) mx_r0402

16,17,54,81,83 SMB_DATA_MAIN
16,17,54,81,83 SMB_CLK_MAIN
SDA SCL

OBSFN_C0 OBSFN_C1 OBSDATA_C0 OBSDATA_C1 OBSDATA_C2 OBSDATA_C3
OBSFN_D0 OBSFN_D1 OBSDATA_D0 OBSDATA_D1 OBSDATA_D2 OBSDATA_D3

GND1 GND2 GND3 GND4 GND5 GND6 GND7 GND8 GND9 GND10 GND11 GND12 GND13 GND14 GND15 GND16 GND17 GND18
NP_NC1 NP_NC2
NC
GND

PEGATRON Title : CPU XDP DEBUG

Pegatron Corp. Engineer: Livy_Zhu

Size	Project Name	Rev
A3	IPMSB-BE/CR	1.00

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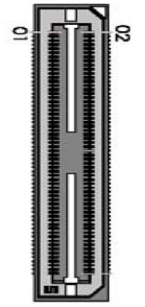
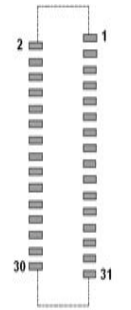
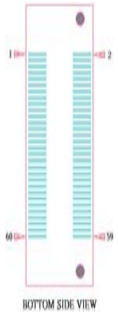
INTEL PCH XDP DEBUG PORT



TOP SIDE VIEW



HRS/DF9C-31S-1V(22)
PCB FOOTPRINT



BOTTOM SIDE VIEW

NOTE:
Place strap resistors of TDO near to XDP connector, and TDI and TMS near to CPU.

NOTE:
Place SR214 near to source in order to avoid stub.

PEGATRON	Title : PCH XDP DEBUG	
Pegatron Corp.	Engineer: Livy_Zhu	
Size: A3	Project Name: IPMSB-BE/CR	Rev: 1.00
Date: Friday, September 24, 2010	Sheet 83 of 83	